17VL013 VERIFICATION METHODOLOGIES

Hours Per Week :

L	T	P	C
4	-	-	4

Total Hours :

L	T	P
60	-	-

WA/RA	SSH/HSH	CS	SA	S	BS
15	30	-	5	5	-

Course Objectives:

- This course gives a brief idea to Hardware Verification methodologies.
- It gives brief idea about Binary Decision Diagrams (BDDs) and algorithms over BDDs.
- It gives introduction to Combinational equivalence checking, Temporal Logics, Modeling sequential systems and model checking, Symbolic model checking.

Course Outcomes:

Upon successful completion of this course student should be able to:

- Able to understand about Hardware Verification methodologies.
- Ability to understand the design of different algorithms over BDDS.
- Able to understand digital systems modeling and equivalence checking.

SKILLS:

- Able to identify combinational equivalence checking.
- Able to implement BDDS from combinational circuits.
- Able to identify the difference between model checking and symbolic checking.

UNIT – I

Introduction to Digital VLSI Design Flow, High Level Design Representation, Transformations for High Level Synthesis

Scheduling, Allocation and Binding

Introduction to HLS: Scheduling, Allocation and Binding, Problem, Scheduling Algorithms, Binding and Allocation Algorithms.

UNIT – II

Logic Optimization and Synthesis Two level Boolean Logic Synthesis, Heuristic Minimization of Two-Level Circuits, Finite State Machine Synthesis, and Multilevel Implementation.

UNIT – III

Verification Introduction to formal methods for verification, Temporal Logic: Introduction and Basic Operators, Syntax and Semantics of CTL, Equivalence between CTL Formulas.

UNIT – IV

Binary Decision Diagram: Introduction and construction, Ordered Binary Decision Diagram, Operations on Ordered Binary Decision Diagram, Ordered Binary Decision Diagram for Sequential Circuits.

UNIT – V

Verification Techniques Introduction to Verification Techniques, Model Checking, Symbolic Model Checking.

ACTIVITIES:

- o For any given problem apply any one of the scheduling algorithm..
- o Design any one of finite state machine.
- o Write a verilog HDL program using basic operators for addition and subtraction.
- o Obtain a OBDD for the given logic function.
- o Write a program for checking the errors in a code using code verification techniques.

TEXT BOOKS:

1. D. D. Gajski, N. D. Dutt, A.C.-H. Wu and S.Y.-L. Lin, High-Level Synthesis: Introduction to Chip and System Design, Springer, 1st edition, 1992.

2. S. Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Prentice Hall,2nd edition, 2003.

REFERENCE BOOKS:

1. G. De Micheli. Synthesis and optimization of digital circuits, 1st edition, 1994.

2. M. Huth and M. Ryan, Logic in Computer Science modeling and reasoning about systems, Cambridge University Press, 2nd Edition, 2004.

3. Bushnell and Agrawal, Essentials of Electronic Testing for Digital, Memory & Mixed-Signal Circuits, Kluwer Academic Publishers, 2000.