17VL011 VLSI SIGNAL PROCESSING

Hours Per Week :

L	T	P	C
3	1	-	4

Total Hours :

L	T	P
45	15	-

WA/RA	SSH/HSH	CS	SA	S	BS
15	30	-	5	5	-

Course Objectives:

- To understand the basic concepts of DSP algorithms.
- To analyze the various pipelining and parallel processing techniques.
- To analyze the retiming and unfolding algorithms for various DSP applications.

Course Outcomes:

- To learn DSP algorithms.
- To understand and analysis the concept of pipelining and other processing for DSP applications.

SKILLS:

- The physical design process of VLSI circuits, including: logic partitioning, floor planning, placement, global routing, detailed routing, clock and power routing, and new trends in physical design.
- Students acquired the knowledge CMOS digital circuits for a low voltage low power environment.
- To impart knowledge on implementation of graph theory in VLSI.

UNIT – I

Introduction to DSP systems-Typical DSP algorithms-Representation of DSP Algorithm - Iteration Bound - Pipelined and parallel processing.

UNIT – II

Retiming - Unfolding –Folding.

UNIT – III

Systolic architecture design -Algorithmic strength reduction in filters and transforms.

UNIT – IV

Pipelined and parallel recursive and adaptive filters- Bit level arithmetic architecture.

UNIT – V

Numerical strength reduction – Overview of low power design and programmable digital signal processors.

TEXT BOOKS:

1. Keshab K.Parthi, " VLSI Digital Signal Processing systems, Design and implementation ",Wiley, Inter Science, 1999.

REFERENCE BOOKS:

1. Mohammed Isamail and Terri Fiez, "Analog VLSI Signal and Information Processing", Mc Graw-Hill, 1994.

2. S.Y. Kung, H.J.White House, T. Kailath, "VLSI and Modern Signal Processing ",Prentice Hall, 1985.

3. Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994

ACTIVITIES:

- To introduce students to the process of designing application specific hardware implementations of algorithms for ASICs (FPGAs).
- Students will work with commercial computer aided design tools to synthesize designs described in hardware description languages by using CAD tools.
- To impart knowledge on automation methods for VLSI physical design.