17VL006 LOW POWER VLSI DESIGN

Hours Per Week :

L	T	P	C
3	1	-	4

Total Hours :

L	T	P
45	15	-

WA/RA	SSH/HSH	CS	SA	S	BS
15	30	-	5	5	-

Course Objectives:

- The student will be able to understand the fundamentals of low power VLSI design.
- In this course, students can study low-power design approaches, power estimation and analysis.
- Another main object of this course is to motivate the graduate students to study and to analyze the low-voltage, low-power adders, Multipliers.
- The concepts of low-voltage, low-power memories and future trend and development of DRAM.

Course Outcomes:

Upon successful completion of this course student should be able to:

- Understand the concepts of low-power design approaches.
- Design and analysis of low-voltage, low-power circuits.
- Extend the low power design to different applications.
- Understand of low-voltage, low-power memories and basics of DRAM.

SKILLS:

- Designing and analyzing skills acquired to words the low power and low voltage circuits.
- Spice circuits simulator usage skills improved.
- Students get skills in developing new techniques to decrement power in existing design for new designs and future use.

ACTIVITIES:

- Write a program for 8 bit addition by using different data types.
- Write a program for 8x1 multiplexer
- Write a program for D flip flop.
- Write a program for shift register.
- Write a program for ALU

UNIT - I

Fundamentals of Low Power VLSI Design: Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT - II

Low-Power Design Approaches: Low-Power Design through Voltage Scaling: VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT - III

Power estimation and analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power and gate level capacitance estimation.

UNIT - IV

Low-Voltage Low-Power Adders, Low-Voltage Low-Power Multipliers Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage, Low- Voltage Low-Power Logic Styles.

UNIT - V

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. Kiat-Seng Yeo, Kaushik Roy, “Low-Voltage, Low-Power VLSI Subsystems”, TMH Professional Engineering.

REFERENCE BOOKS:

1. Kaushik Roy, Sharat C. Prasad, “Low Power CMOS VLSI Circuit Design”, John Wiley & Sons, 2000.

2. Gary K. Yeap, “Practical Low Power Digital VLSI Design”, Kluwer Academic Press, 2002.