17VL003 DIGITAL IC DESIGN

Hours Per Week :

L	T	P	C
3	-	3	5

Total Hours :

L	T	P	WA/RA	SSH/HSH	CS	SA	S	BS
45	-	45	15	30	-	5	5	-

Course Objectives:

- To learn the basic MOS Circuits
- To learn the MOS Process Technology
- To understand the operation of MOS devices.
- To impart in-depth knowledge about analog and digital CMOS circuits.

Course Outcomes:

Upon successful completion of this course student should be able to:

- Analyse the operation of CMOS.
- Analyse the design rules and layout diagram.
- Design of low power Adders and Multipliers.
- Analyse the physical design process of VLSI design flow.
- Design of CMOS Memories.

SKILLS:

- The ability of taking decision over the design aspect of digital IC for a particular application increases.
- Skill of Designing new techniques for critical parameters in digital IC design like power is improved.
- Circuit and switch level simulation and verification in design tool skill acquired.

UNIT – I

CMOS Inverter: Introduction to MOS transistor, V-I Characteristics, Electrical Parameters, Static behaviour, switching Threshold, Noise Margins, Robustness revisited, Dynamic behaviour: Computing the capacitances, propagation delay, propagation delay from a design perspective, power,energy and energy delay.

UNIT – II

Combinational Logic Design: Introduction, Static CMOS Design: Complementary CMOS, ratioed logic, pass transistor logic dynamic CMOS Design: Dynamic logic, speed and power dissipation of dynamic logic, signal integrity issues in Dynamic design, cascading dynamic gates.

UNIT – III

Sequential Logic Design: Introduction, static latches and registers: The Bistablility principle, multiplexer based laches, master-slave edge-Triggered register, low-voltage static laches, Static SR Flip-flop, dynamic laches and registers, dynamic transmission, Gate Edge - triggered registers, CMOS NORA-CMOS True single - phase clocked register (TSPCER).

UNIT – IV

Timing Issues in Digital Circuits: Introduction, Timing classification of digital systems, synchronous design, Self-Timed circuit design, synchronizers and arbiters.

UNIT – V

Digital Integrated System Building Blocks: Introduction, Adders, Multipliers, Shifters, Memories, ROM, RAM, Internal structure, ROM 2 D Structure, SRAM, DRAM.

DIGITAL IC DESIGN LAB

List of Experiments

1. Design of Inverter and all logic gates
2. Design and Simulation of Full adder
3. Design and Simulation of Serial Binary Adder, Carry Look Ahead Adder.
4. Design of SRAM and DRAM
5. Design of pseudo logic gates
6. Design of DCVSL logic gates
7. Design of flip flops: SR, D, JK, T
8. Design of edge triggered registers
9. Design of barrel shifter
10. Design of Multiplier

Note: Implementing the above designs on Circuit level/ RTL level in Cadence/Xilinx.

ACTIVITIES:

- *Discussing different case studies like real design examples*
- *Implementing existing design tool and verifying the response of that particular design IC.*
- *Taking a particular design and doing all steps in VLSI design flow.*

TEXT BOOKS:

1. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic., Digital Integrated Circuits: A Design Perspective, Second Edition, **Pearson Education India,** 2003
2. Ken Martin, Digital Integrated Circuit Design, Oxford University Press, 1st edition, 1999.

REFERENCE BOOKS:

1. Neil H. E. Weste and D. M. Harris, CMOS VLSI Design, Third Edition, 2010. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.