17ES014 DSP PROCESSORS

Hours Per Week :

L	T	P	C
3	1	-	4

Total Hours :

L	T	P
45	15	-

WA/RA	SSH/HSH	CS	SA	S	BS
15	30	-	5	5	-

Course Objectives:

Digital Signal Processing (DSP) is being used very widely in applications that include telecommunication equipment, multimedia systems, electronic and biomedical instrumentation, automotive systems and many military and weapon systems. DSP chips, general processors or dedicated ASIC chips, are now able to process wide bandwidth signal of all sorts in real-time.

- Architecture of a Real time Signal Processing Platform
- Digital Signal Processor Architecture
- Difference in the complexity of programs between a General PurposeProcessor and Digital Signal Processor
- Apply previous signal processing knowledge in real-time digitalsignal processing systems.
- Learn to program a DSP processor.
- Prepare students with multi disciplinary competency

Course Outcomes:

- Design digital signal processor (DSP)
- Comprehend performance enhancements provided by DSP in theareas: memory architecture, pipelining, parallel execution, cache use, direct memory access, addressing methods, hardware loop control etc.
- Different Errors introduced during A-D and D-A converter stage
- Develop tools and methods for DSP.

SKILLS :

- Knowledge of signals and systems, convolution methods, digital signal processing concepts must be known.

ACTIVITIES:

- Implementation of CODEC interface circuit
- Implementation of sensors with DSP Processors
- FFT implementation on DSP Processor.

UNIT – I **L-09**

ARCHITECTURES FOR PROGRAMMABLE DIGITAL SIGNAL PROCESSING DEVICES: Introduction, Basic Architectural Features, DSP Computational BuildingBlocks, Bus Architecture and Memory, Data Addressing Capabilities, AddressGeneration Unit, Programmability and Program Execution, Speed Issues, Features for External Interfacing.

UNIT – II **L-09**

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS : Introduction, Commercial Digital Signal-processing Devices, Data AddressingModes of TMS320C54xx Digital Signal Processors, Data Addressing Modesof TMS320C54xx Processors, Memory Space of TMS320C54xx Processors,Program Control.

UNIT – III **L-09**

DSP PROGRAMMING AND OPERATIONS : TMS320C54xx Instructions and Programming, Programming for IIR, FIR, FFTetc., On-Chip peripherals, Interrupts of TMS320C54xx Processors, PipelineOperation of TMS320C54xx Processors.

UNIT – IV **L-09**

INTERFACING MEMORY AND PARALLEL I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES: Introduction, Memory Space Organization, External Bus Interfacing Signals,Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I/O, Direct Memory Access (DMA)

UNIT – V **L-09**

INTERFACING SERIAL CONVERTERS TO A PROGRAMMABLE DSP DEVICE : Introduction, Synchronous Serial Interface, A multi-channel Buffered SerialPort (McBSP), McBSP Programming, A CODEC Interface Circuit, CODECProgramming, A CODEC-DSP Interface Example.

TEXT BOOKS:

1. Lapsley et al., “DSP Processor Fundamentals, Architectures & Features”, S. Chand & Co, 2000.
2. “Digital Signal Processing”, A. Singh & S. Srinivasan, Thomson Learning.

REFERENCE BOOKS:

1. B. VenkataRamani and M. Bhaskar, “Digital Signal Processors, Architecture, Programming and Applications”, TMH, 2004.
2. Jonatham Stein, “Digital Signal Processing”, John Wiley, 2000
3. Embedded Dsp Processor Design Application Specific Instruction Set Processorsby LiuShroff (2008)