16EC305 COMPUTER ARCHITECTURE AND ORGANIZATION

Hours Per Week :

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3	-	-	3

Course Description and Objectives:

The objective of this course is to analyze architectures and computational designs, understand various conventional computational organizations. This course covers a number of issues involved in the design and utilization of high performance computing systems, including Instruction Set, Architecture, Performance Evaluation, Pipelining, Memory, Multiprocessor and Parallel Computing and Interconnection Network.

Course Outcomes:

Upon successful completion of this course, students should be able to:

CO1: Understand the basic structure and operation of a digital computer.

CO2: Apply arithmetic algorithms and interpret the processed data.

CO3: Understand and analyze the concepts of CPU and its operations.

CO4: Categorize various memory mechanisms.

CO5: Understand and comparevarious data transfer techniques.

CO6: Understand the design of a pipelined, array and multiprocessors.

UNIT - 1 **L-9**

INTRODUCTION: Introduction to organization and architecture, Brief history of computers, A Top-level view of computer function and interconnection - Computer components, Computer function, Interconnection structures, Bus interconnection, PCI.

UNIT - 2 **L-9**

CENTRAL PROCESSING UNIT: Computer arithmetic - Integer arithmetic, Floating-Point representation, Floating-Point arithmetic; Instruction sets - Machine instruction characteristics, Types of operands, Types of operations; Instruction sets - Addressing modes, Instruction formats; Processor structure and function - Processor organization, Register organization, Stack organization and Instruction cycle; Control unit operation - Micro-Operations, Control of the processor, Hardwired implementation; Basic concepts of micro programmed control.

UNIT -3 **L-9**

MEMORY: Internal memory - Computer system memory overview, Semiconductor main memory, Cache memory, Virtual memory; External memory - Magnetic disk, RAID, Magnetic tapes, Flash memory.

UNIT - 4 **L-9**

INPUT / OUTPUT: External devices, I/O modules, Programmed I/O, Interrupt driven I/O, DMA, I/O channels and processors.

UNIT - 5 **L-9**

PIPELINE, VECTOR PROCESSING AND MULTIPROCESSORS: Pipeline and vector processing - Parallel processing, Pipelining, Arithmetic pipeline, Instruction pipeline, RISC pipeline vector processing, Array processors; Multiprocessors - Characteristics of multiprocessors, Interconnection structures, Inter processor communication and synchronization, Cache coherence.

TEXT BOOKS:

1. William Stallings, “Computer Organization and Architecture”, 9th edition, Pearson/PHI, 2013.
2. M.Moris Mano, “Computer Systems Architecture”, 3rd edition, Pearson/PHI, 2013.

REFERENCE BOOKS:

1. Carl Hamacher, Zvonko Vranesic and Safwat Zaky, “Computer Organization”, 5th edition, TMH, 2011.
2. John P.Hayes, “Computer architecture and Organization”, 3rd edition, Tata McGraw-Hill, 1998.
3. P.Pal Chaudhuri, “Computer organization and design”, 3rd edition, Pearson/PHI, 2008.
4. G.Kane and J.Heinrich, “MIPS RISC Architecture”, 2nd edition, Pearson/PHI, Prentice Hall, 1992.