SECOND GENERATION DIFFERENTIAL CURRENT CONVEYOR (DCCII) AND ITS APPLICATIONS

A THESIS

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Dedicated

to

My Late Grand Parents
Vallabhuni Rama Rao & Rukhminamma

DECLARATION

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This is to certify that the thesis entitled **SECOND GENERATION DIFFERENTIAL CURRENT CONVEYOR (DCCII) AND ITS APPLICATIONS** submitted by **VALLABHUNI VIJAY** to the Vignan's Foundation for Science, Technology and Research University, Vadlamudi, Guntur, for the award of the degree of **Doctor of Philosophy** is a bonafide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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Place: Guntur
Date: July 2017

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ABSTRACT

SECOND GENERATION DIFFERENTIAL CURRENT CONVEYOR (DCCII) AND ITS APPLICATIONS

Square wave generators are facing vital role in many electronic applications as a reference input for analog signal handling functions. Those are, in specifically, communication equipments, control modules, signal dispensation appliances, measurement blocks, feedback control circuits for power conversion mechanism, based on operating frequency range used in sensor interfaces, telecommunications and clock for digital structures. All these prerequisites are fulfilled with the operational amplifier (OA) based classic square wave generator. Conversely, OAs has the snag of lower operating frequencies as it bears from lower slew rate and flat gain bandwidth product limitation.

Integrated continuous time filters are now widely accepted in industry where they are used in applications involving direct signal processing especially for medium dynamic range applications in cases where high speed and/or low power dissipation are needed. Recently, current mode (CM) approach has attracted much attention in analogue circuit design due to its overindulgence merits to that of OAs. Rapid exploration of CM design, mechanisms and advancements, offering improved bandwidth, maximum slew rate, cleanness of circuit design and realization, enhanced linearity, reduced power consumption, better dynamic range, easiness in execution of a range of functions with minimum additional passive components. The DCCII is a suitable building block for the realization of current mode applications. By considering the advantages offering in CM circuits and to meet the need for generating square wave generator circuit and all pass filter circuits in most electronic appliances, some new square wave generators and all pass filter circuits are proposed in this thesis.

Although current mode filters can be implemented in the voltage mode using OAs, they usually suffer from the finite gain-bandwidth product of the OAs which limits the frequency range. In this thesis, new all-pass filters with the DCCII as the main active device are proposed. The proposed circuits consist of two resistors and two capacitors, including one grounded capacitor, suitable for tuning. In literature, it is

widely accepted that use of grounded capacitors makes the designs suitable for integrated circuit (IC) realisation. Grounded IC capacitors have less parasitics compared to floating counterparts, which is important from the performance point of view and to avoid noise effects. Furthermore, the floating capacitors require an IC process with two poly layers. The performance evaluation of the proposed circuit vis-à-vis existing all-pass sections is carried out. The simulation of the circuit is done using SPECTRE simulation-model parameters. Experimental results of the proposed design using AD844AN ICs (commercially available current feedback operational amplifier (CFOA)) are included, which conform to the simulation results.

KEYWORDS: All-pass filter, Current mode and voltage mode device, Duty Cycle, Linearity, Noise effect, Oscillators, Second Generation Differential Current Conveyor, Signal processing, Square Wave Generators, Voltage Cascading Applications.

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LIST OF SYMBOLS AND ABBREVIATIONS

ω	Angular Frequency, rad/s
ABB	Active Building Block
APF	All-Pass Filter
BD-QFG	Bulk Driven and Quasi Floating Gate
C-(I)CDBA	Current-controlled (inverting) current differencing buffered amplifier
CC	Current Conveyor
CC-CDBA	Current Controlled Current Differencing Buffered Amplifier
CCCDTA	Current Controlled Current Differencing Transconductance Amplifier
CCI	First-Generation Current Conveyor
CCCII-	Minus-type second-generation current controlled current conveyor
CCII	Second-Generation Current Conveyor
CCII+(-)	Plus-type (minus-type) second-generation current conveyor
CCIII	Third-Generation Current Conveyor
CCIII-	Minus-type third-generation current conveyor
CDBA	Current Differencing Buffered Amplifier
CDTA	Current Differencing Transconductance Amplifier
CFOA	Current Feed-Back Operational Amplifier
CM	Current Mode
CS	Current Subtractor
CMOS	Complementary Metal Oxide Semiconductor
DCC	Differential Current Conveyor
DCCCS	Differential Current Controlled Current Source
DCCII	Second Generation Differential Current Conveyor
DDCC+	Plus-type differential difference current conveyor
DO-CCII	Dual-output second-generation current conveyor

DRC	Design Rule Checker
DVCC	Differential Voltage Current Conveyor
DVCC+	Plus-type differential voltage current conveyor
DXCCII	Dual-X Second-Generation Current Conveyor
FDCCII	Fully Differential Current Conveyor
FDNR	Frequency-Dependent Negative Resistance
FTFN	Four Terminal Floating Nuller
GDSII	Graphical Data Stream Information Interchange
IAFCCM	Improved Active-Feedback Cascode Current Mirror
IC	Integrated Circuit
ICCII	Inverting Second Generation Current Conveyor
JFET	Junction Field Effect Transistor
KCL	Kirchhoff's Current Law
LVS	Layout Vs Schematic
MCCII-	Minus-type modified second-generation current conveyor
MDCC	Modified Differential Current Conveyor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MRC	MOS resistive circuits
OA	Operational Amplifier
OTA	Operational Transconductance Amplifier
OTRA	Operational Transresistance Amplifier
RF	Radio Frequency
RHP	Right-Half Plane
RNMC	Reversed Nested Miller Compensation
SSF	Super Source Follower
UVC	Universal voltage conveyor

VM	Voltage Mode
VM-ABB	Voltage Mode Active Building Block
VCVS	Voltage Controlled Voltage Source
VDTA	Voltage Differencing Transconductance Amplifier
VDBA	Voltage Differencing Buffered Amplifier
VD-DIBA	Voltage differencing-differential input buffered amplifier
VLSI	Very Large Scale Integration

CHAPTER I

INTRODUCTION AND BACKGROUND

1.1. Introduction

In general, Square wave generators are facing vital role in many electronic applications as a reference input for analog signal handling functions. Those are, in specifically, communication equipments, control modules, signal dispensation appliances, measurement blocks, feedback control circuits for power conversion mechanism, based on operating frequency range used in sensor interfaces, telecommunications and clock for digital structures (J.M. Jacob et al, 2000, S. Franco et al, 2002). All these prerequisites are fulfilled with the operational amplifier (OA) based classical square wave generator (J.M. Jacob et al, 2000). Conversely, OAs has the snag of lower operating frequencies as it bears from lower slew rate and flat gain bandwidth product limitation (H.C. Chien, 2012).

For the last two decades, because of the advantages of high performance and versatility all the electronic applications are being designed using current mode (B. Dalibor et al, 2008). The inevitable reasons for switching from voltage mode to current mode are high slew rate, improved dynamic range, better bandwidth, easiness in circuit realization, power reduction (K.K. Abdalla et al, 2012), (M. Akbari et al, 2015). The waveform generator proposed using Operational transconductance amplifier (OTA) in S.K. Kar et al, 2011, used more active elements in addition to that of possession of more passive components causes more power consumption and occupies even more area besides the advantages of grounded capacitor feature offered. The circuit in A.D. Marcellis et al, 2013 has used only a couple of active elements, but uses seven passive components and also not offering the grounded capacitor. Given circuits in R. Pal et al, 2015, H.C. Chien et al, 2014, S. Malik et al, 2015, A. Srinivasulu et al, 2016, S. Minaei et al, 2012 consists of same glitch of usage of higher number of passive and active devices causes the circuit usage limited to less in IC fabrication. In order to make the circuit simpler and designer's choice by using only one active and minimum possible usage of passive components with maximum reduction of noise effects and parasitics in designing a waveform generator, a new CM current differencing device is designed.

All-pass filter is a special mode of frequency selective circuit which allows all the frequencies by maintaining the equal levels of amplitude with variation in the produced phase in accordance to the input signal. High input impedance feature is the primary requisition for making an all-pass filter used in voltage mode (VM) applications, where employed for phase compensation requirement. Additional provision of phase compensation network removes the need for voltage buffering circuit or current conveyor (CC).

1.2. Introduction to Current–Mode and Voltage–Mode Circuits

Numerous well-known advantages of current-mode (CM) circuits such as high bandwidth, greater linearity, low voltage operation, and wide dynamic range are made them popular in the fields of analog signal processing and integrated circuit design (K. C. Smith, 1968, G. Palmisano et al, 1999, Y.S. Hwang et al, 2009, R. Senani et al, 2015, F. Lin et al, 2015). In the open technical literature excessive number of CM circuits exist that promote solutions to a wide spectrum of applications. For an instance works (D. Biolek et al, 2008, D. Prasad et al, 2010, A.U. Keskin et al, 2005, M. Atasoyu et al, 2015, E.T. Cuautle et al, 2013, H.O. Elwan et al, 1996, S. Ciftcioglu et al, 2005, B. Metin et al, 2012, B. Metin et al, 2012, S. Shahsavari et al, 2015, A. Toker et al, 2000) and references cited therein can be mentioned. Over the last decades a significant research was performed in order to design high performance, low-voltage low-power CM circuits mainly due to the requirement of efficient portable electronic systems with long battery lifetime (E.T. Cuautle et al, 2013, H.O. Elwan et al, 1996, S. Ciftcioglu et al, 2005, B. Metin et al, 2012a, B. Metin et al, 2012b, S. Shahsavari et al, 2015, A. Toker et al, 2000, A. K. Kafrawy et al, 2009, E. Arslan et al, 2013, S. Minaei et al, 2013, W. Tangsrirat et al, 2006, F. Kacar et al, 2011, C. Cakir et al, 2010, O.G. Sokmen et al, 2015). Square wave generators are extensively used in ample range of applications in the vein of analogue signal applications viz. Voltage controlled duty cycle oscillator in silicon sensors, A/D and D/A converters, for external tuning of pulse width modulation in control modules, calibration systems, applied electronics, communication modules, electronic-instrumentation, signal processing functions, control circuits to power converting mechanism, based on range of operating frequency used in sensor interfaces, telecommunications and switching networks, clocking pulse in digital systems, electromechanical systems (M.T. Abuelma'atti et al, 2004, W.W. Cheng et al, 1985,

D. Pal et al, 2009, R.R. Spencer et al, 1990, S. Siskos et al, 1992, A.K.M.S. Haque et al, 2008, B. Wilson et al, 1990, A. Srinivasulu et al, 2016). This rationalizes the enlargement of a hefty quantity of square wave generators using a diversity of circuit configurations (S.I. Liu et al, 1993). All these circuits are initially developed with the most readily available active element of the voltage mode operational amplifier. Regrettably, operational amplifiers have some drawbacks; specifically with regards to lower gain bandwidth product and lower operating frequency hitch (J.M. Jacob et al, 2000).

Recently in contrast to voltage mode devices eccentric approach of the current mode (CM) technology has been adopted to design all electronic applications due to their high performance and versatility (C. Toumazou et al, 1990, M.O. Cicekoglu et al, 1998, B.N. Ray et al, 2004, S.J.G. Gift et al, 2005, D. Pal et al, 2009, Y.K. Lo et al, 2007). The advantages offered by CM circuits are specific, with improved accuracy, finer slew rate, advanced bandwidth, easy to realize with externally joined passive components, its simplicity of implementation, uncomplicated circuitry, less-power utilization (C.L. Hou et al, 2005, P. Silapan et al, 2011, A.U. Keskin et al, 2004, Y.H. Ghallab et al, 2005, J. Jerabek et al, 2015, R. Sotner et al, 2015, H. Kim et al, 2007, R. Sotner et al, 2013, M. Koksal et al, 2008, R. Sotner et al, 2013, H.C. Chien et al, 2011). These square wave generators are enduring from designs with an excessive number of active elements, too much usage of capacitors or resistors, lack of electronic tunability due to possession of floating variable resistors used to control frequency, incongruous for high frequency operations.

Integrated continuous time filters are now widely accepted in industry (R.H. Zele et al, 1993, A.M. Durham et al, 1993) where they are used in applications involving direct signal processing especially for medium dynamic range applications in cases where high speed and/or low power dissipation are needed. The DCCII is a suitable building block for the realization of current mode filters. Although current mode filters can be implemented in the voltage mode using op-amps, they usually suffer from the finite gain-bandwidth product of the op-amps which limit the frequency range. With the inclusion of several high performance VM active building blocks (VM-ABBs) (B. Metin et al, 2012, R.I. Salawu et al, 1980, B. Metin et al, 2003, I.A. Khan et al, 2000, N. Pandey et al, 2004, M. Higashimura et al, 1988, B. Metin et al, 2009, E. Yuce et al, 2010, B. Metin et al, 2011, M.A. Ibrahim et al, 2011,

S. Maheshwari et al, 2011, S. Maheshwari et al, 2010, H.O. Elwan et al, 1996, C. Acar et al, 1999, A. Sedra et al, 1970), many different forms of APFs are proposed in the literature. Each ABB has its own advantage because of their design consideration and internal circuit constraints. An APF is designed with second-generation current conveyor (CCII) and a grounded capacitor in (R.I. Salawu et al, 1980). The disadvantage in (R.I. Salawu et al, 1980) is not-so-high input impedance and use of three resistors in (B. Metin et al, 2003). The all-pass filters using third-generation current conveyor (CCIII) suffers from the unavailability of grounded capacitor. Also, they are not useful for cascading with other filters (I.A. Khan et al, 2000, N. Pandey et al, 2004). Even though the all-pass filters in (M. Higashimura et al, 1988) are designed using the inverted second generation current conveyor (CCII-) with high input impedance, it has the disadvantage of floating capacitor and require additional passive components. The all-pass filters realized with dual output CCII (DO-CCII) and CCII (B. Metin et al, 2009, E. Yuce et al, 2010) offers both high-input impedance and grounded capacitor but do not result in low output impedance. The all-pass filters of (E. Yuce et al, 2010, B. Metin et al, 2011, M.A. Ibrahim et al, 2011, S. Maheshwari et al, 2011, S. Maheshwari et al, 2010, B. Metin et al, 2011) have the advantage of both high-input impedance and grounded capacitor, although only (E. Yuce et al, 2010, M.A. Ibrahim et al, 2011, S. Maheshwari et al, 2011, S. Maheshwari et al, 2010) have low-output impedance. The advantage of providing all three desired features is dominated by designs using double active elements like differential voltage current conveyor (DVCC) and differential difference current conveyor (DDCC) or as in (S. Maheshwari et al, 2010 and B. Metin et al, 2011), designs using a second generation fully differential current conveyor (FDCCII). Even the circuits in M.A. Ibrahim et al, 2011, S. Maheshwari et al, 2011 provides the desired features but all three resistors used were in grounded form.

1.3. Thesis Objectives

From internal structure implementation point of view, the current subtractor (CS) with current differencing capability (C.W. Lin et al, 2011, E. Arslan et al, 2013) forms one of the most important sub-stages of recently proposed high-performance CM active building blocks (ABBs) such as current differencing transconductance amplifier (CDTA) (D. Biolek et al, 2008, D. Prasad et al, 2010, F. Kacar et al, 2011), current differencing buffered amplifier (CDBA) (A.U. Keskin et al, 2005, A. Toker et

al, 2000, W. Tangsrirat et al, 2006, C. Cakir et al, 2010), operational transresistance amplifier (OTRA) (Y.S. Hwang et al, 2009, A.K. Kafrawy et al, 2009), or second-generation differential current conveyor (DCCII) (H.O. Elwan et al, 1996, S. Ciftcioglu et al, 2005, B. Metin et al, 2012, B. Metin et al, 2012, S. Shahsavari et al, 2015). Although the DCCII element was the first active component in the open literature combining the simplicity of the conventional CCII (K.C. Smith et al, 1968) with current differencing attribute of the conventional CDBA (A.U. Keskin et al, 2005), it has not received as much attention as the CDBA yet and up to now only few integrated circuit implementations are available (H.O. Elwan et al, 1996, S. Ciftcioglu et al, 2005, B. Metin et al, 2012a, B. Metin et al, 2012b). In order to show versatility of DCCII and increase its importance for analog signal processing, recently it was used as the main sub-block in a frequency compensation scheme of three stage amplifier (S. Shahsavari et al, 2015). It is well-known in analog circuit design that reduction of unwanted parasitic terminal capacitance and resistance values increase the bandwidth of a circuit, because of the product of these two quantities form a dominant pole. In accordance with this theory, within this thesis novel CMOS implementation of a low-voltage and low-power high performance DCCII based waveform and filter circuits are proposed. Differential current conveyor (DCCII) can be defined as a second-generation current conveyor with current differencing capability. By possessing these advantages of DCCII and need for square wave generators in electronic applications, some novel circuits with two resistors and a single capacitor for square wave generation using DCCII as an active element is highlighted.

In literature, it is widely accepted that use of grounded capacitors makes the designs suitable for integrated circuit (IC) realization. Grounded IC capacitors have less parasitics compared to floating counterparts, which is important from the performance point of view and to avoid noise effects. Furthermore, the floating capacitors require an IC process with two poly layers. Integrated continuous time filters are now widely accepted in industry (R.H. Zele et al, 1993, A.M. Durham et al, 1993) where they are used in applications involving direct signal processing especially for medium dynamic range applications in cases where high speed and/or low power dissipation are needed. The DCCII is a suitable building block for the realization of current mode filters. Although current mode filters can be implemented in the voltage

mode using OAs, they usually suffer from the finite gain-bandwidth product of the op-amps which limit the frequency range. In this thesis, new all-pass filters with the Differential Current Conveyor (DCCII) as the main active device are proposed. The proposed circuits consist of two resistors and two capacitors, including one grounded capacitor, suitable for tuning. The performance evaluation of the proposed circuit vis-à-vis existing all-pass sections is carried out. The simulation of the circuit is done using SPECTRE simulation-model parameters. Experimental results of the proposed design using AD844AN ICs are included, which conform to the simulation results.

1.4. Organization of Thesis

Chapter (2) deals with an introductory overview of the second generation differential current conveyor (DCCII) and its CMOS implementation. Eleven CMOS DCCII implementations are discussed in this chapter. These CMOS DCCII implementations are already reported in (H.O. Elwan et al, 1996, Cevdet Acar et al, 1999, A. Sedra et al, 1970, H. Hesham et al, 2001, Ç. Sinem et al, 2005, G. Ferri, 2006, F. Kacar, 2010, R. Chavoshisani, 2011, A. Sallem et al, 2011, B. Metin, 2012, A. Sallem, 2012, B. Metin, 2013, S. Shahsavari, 2014, J. Koton, 2014, M. Kumngern, 2014, S. Shahsavari, 2015, E. Arslan, 2016). Two of these CMOS DCII implementations are based on the Bi-CMOS technique. The DCCII implemented with second generation current conveyor (CCII) followed by a current subtractor is discussed. One DCCII is based on BD-QFG methodology. Using differential current conveyor another DCCII is proposed. The DCCII implemented using DXCCII is also given. The operation of these eleven DCCIIs is studied and their merits and drawbacks are discussed and elaborated.

Chapter (3) provides the background review of the existed all-pass filters, band-pass filters, multiple output filter, current comparator, inductance simulator, four quadrant multiplier and frequency comparator circuits DCCII. Three all-pass filter circuits amongst two are voltage mode and one is current mode all pass filter are discussed. One band pass filter also given. Nine inductance simulator circuits are presented. Two multiplier blocks are mentioned with inclusion of single application of frequency comparator, frequency dependent negative resistant circuit and current comparator is elaborated in this chapter. The advantages of these circuits are quoted and their drawbacks are given in this chapter.

Chapter (4) introduces some novel waveform generator circuits and all pass filter circuits. By using two resistors and a single capacitor with second generation differential current conveyor (DCCII) as an active element some new square wave generators are proposed and implemented and mathematical analysis of the proposed circuits is also given. The operations of the proposed circuits to produce oscillations are discussed in detail. The basic network laws and ideal terminal characteristics of DCCII are applied to the proposed circuits to derive the oscillation frequency and circuits realized. Similarly, the same procedure is applied to derive the mathematical equations for the all pass filter circuits.

Chapter (5) deals with the simulation results of the proposed circuits in chapter (4). All the proposed circuits are checked for waveform generation by connecting with passive components. The passive component values are calculated from the mathematical equations derived in chapter (4). All the proposed circuits are simulated using Cadence Spectre simulation model parameters. And the simulation results are presented in this chapter to validate the corresponding mathematical analysis carried out in chapter (4).

Chapter (6) presents hardware implementation of the proposed circuits on a laboratory bread board. The DCCII prototype circuit is implemented by using two AD844 AN ICs and external passive components are connected to test the waveform generation of the proposed circuits. The proposed circuits are tuned for different passive component values. Hardware results are given in this chapter to validate the simulation and theoretical analysis.

Chapter (7) presents the advantages of the proposed circuits compared to the existing circuits in the literature based on OTRA. And finally conclusions and future scope are given in this chapter.

CHAPTER II

SECOND GENERATION DIFFERENTIAL CURRENT CONVEYOR (DCCII)

2.1. Introduction

The first generation current conveyor (CCI) was presented by Sedra and Smith in 1968. They presented the second generation current conveyor in 1970. However, a certain work to show that the current conveyor was a more advantageous device than the operational amplifier, couldn't be done during following ten years. So, the current conveyor has been a conceptual device until early 1980s. After innovations in integrated circuit (IC) technology it is that the current conveyor can be realized in ICs. In the result of these works, it was understood that the circuits which are implemented by using CCIIs have their own advantages. Generally, many circuit blocks can be implemented using CCIIs which is easier than implementation using Op-Amps.

The differential current conveyor (DCCII) is a powerful current-mode building block with properties that make it very suitable for designing all-MOS analog circuits which can be integrated on a single chip. The proposed analog block is an extension to the second generation current conveyor presented by Sedra and Smith (A. Sedra et al, 1970). Although the CCII can be used for the realization of many analog functions, the circuits employing the CCII often rely on floating resistors and capacitors which, when integrated on the chip, bring many problems associated with parasitics, area consumption, temperature dependency, etc. The presented differential current conveyor, on the other hand, can be used with MOS transistors operating in the ohmic region to implement the required analog functions where the even and in some cases the odd nonlinearities associated with the transistors operating in this mode can be cancelled out.

2.2. CMOS Second Generation Differential Current Conveyor (DCCII)

The DCCII representation of inputs and outputs with corresponding current direction is shown in Figure 2.1. DCCII is a four terminal device among Y, X_P and X_N drives, input and the remaining Z terminal serve as output. The fundamental property of DCCII is current differencing, which is reflected across Z for the input current flowing across X_P and X_N. Furthermore, it offers a high input impedance feature which

plays a vital role in the voltage cascading applications, is driven by terminal *Y* across the input. The potential applied across *Y* terminal is being copied to the other input terminals of X_P and X_N.

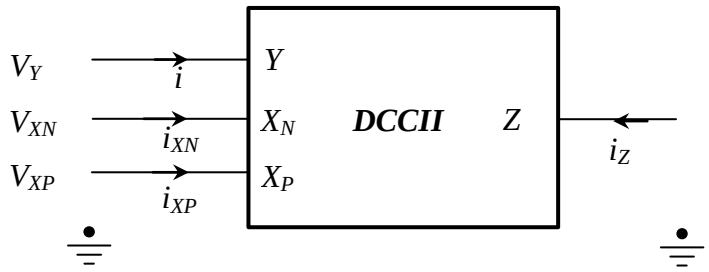


Fig. 2.1. Emblematic depiction of the DCCII input and output terminal currents and voltages.

The hybrid matrix of input and output terminal relation to ideal parameter consideration is presented in (1).

$$\begin{bmatrix} V_{XN} \\ V_{XP} \\ i_Z \\ i_Y \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & 1 \\ 1 & -1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{XP} \\ i_{XN} \\ V_Y \end{bmatrix} \tag{1}$$

From (1), it has been observed that the output current i_Z, is reflected as the difference of input currents X_N and X_P, respectively. Along with the same input potential at the *Y* is driving across the remaining two inputs of X_P and X_N without passing any current through it.

The behavioral model of the DCCII active element is given in Figure 2.2.

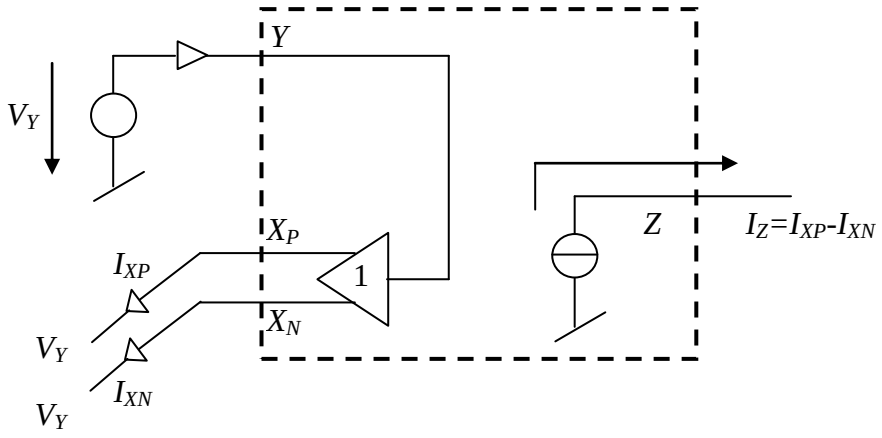


Fig. 2.2. Behavioral model of the DCCII.

2.2.1. Hassan O. Elwan DCCII, 1996

The differential current conveyor (DCC) is a five terminal analog building block as shown in Figure 2.3 with a describing matrix of the form

$$\begin{bmatrix} V_{X_1} \\ V_{X_2} \\ I_{Z_1} \\ I_{Z_2} \\ I_Y \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 \\ 1 & -1 & 0 & 0 & 0 \\ -1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{X_1} \\ I_{X_2} \\ V_{Z_1} \\ V_{Z_2} \\ V_Y \end{bmatrix} \tag{2}$$

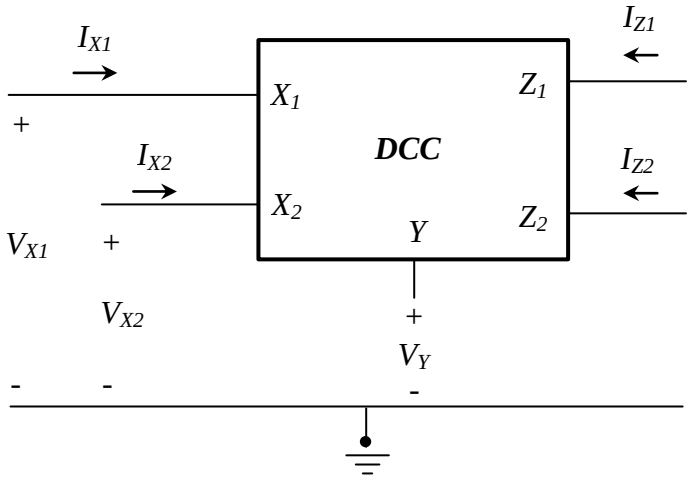


Fig. 2.3. The differential current conveyor.

The MOS realization of the DCC is shown in Figure 2.4. All transistors are assumed to be operating in the saturation region with the sources connected to their substrates. The *Y* terminal voltage is applied to the gate of transistor M_1 along with M_2, which forms a CMOS pair. The current through this pair is mirrored by M_3, M_4 and M_8 to the CMOS pairs formed by M_5, M_6 and M_{12}, M_{13} since the gate voltage of M_2, M_5 and M_{12} are the same therefore:

$$V_{X_1} = V_{X_2} = V_Y \tag{3}$$

The negative feedback operation of the transistors M_7 and M_9 with the bias currents flowing through transistors M_{10} and M_{11} ensure that the voltage at X_1 and X_2 remain independent of the current withdrawn from the X terminals. The difference between X_1 and X_2 currents is conveyed to the Z_1 terminal by the mirroring action of transistors M_{14}, M_{15} and the current mirror formed by transistors M_{18}, M_{19}. The inversion of this current is obtained at the Z_2 terminal by repeating the above circuit with interchanged current mirror transistors.

The above analysis assumes that the sources of the transistors are connected to their substrates. This is necessary, in order to make the threshold voltage constant for all the transistors, however this requires that, the NMOS transistors and the PMOS transistors be separable in different wells. Although twin well CMOS technology is available, it is not a standard VLSI technology. Another disadvantage is that the use of separate wells increases the layout area because every time separate wells are used, guard rings have to surround each well to prevent latch-up.

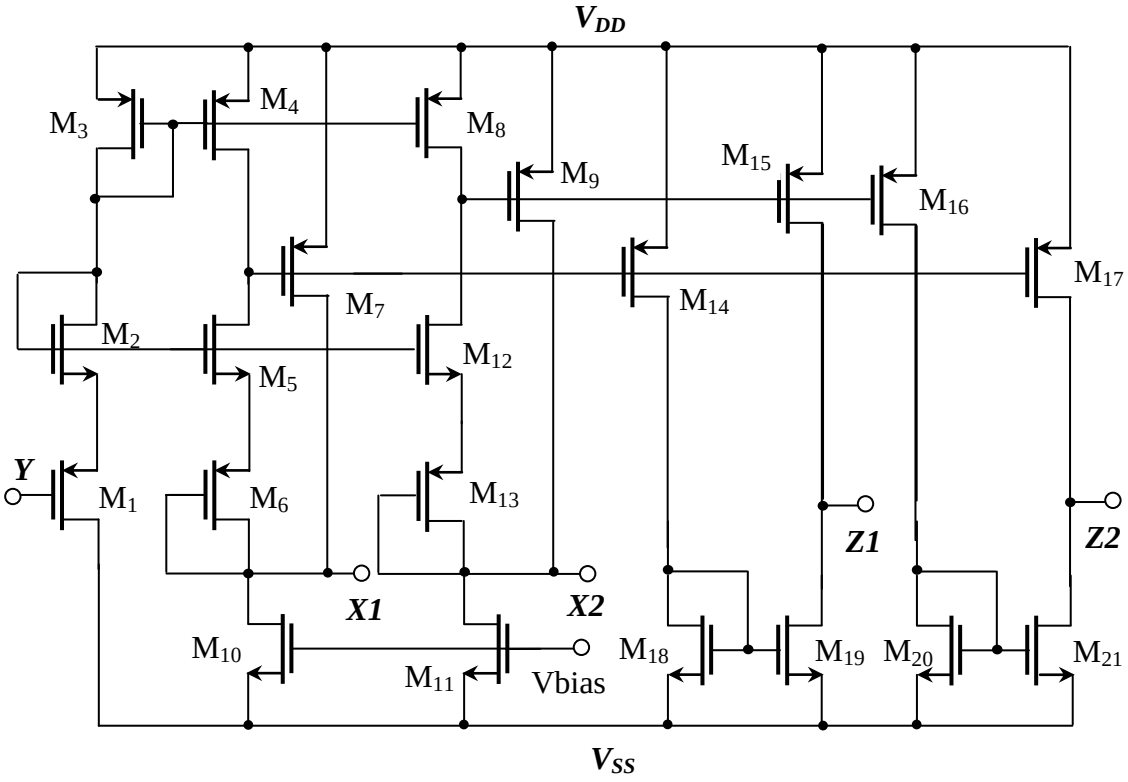


Fig. 2.4. The DCC Circuit realization (H.O. Elwan et al, 1996).

2.2.2. Firat Kacar DCCII, 2010

The DXCCII is conceptually a combination of the regular CCII (T. Kurashina et al, 1998) and the inverting current conveyor (ICCII) (H. Traff et al, 1992). The DXCCII symbol is illustrated in Figure 2.5. It has two X terminals, namely X_p (non-inverting X terminal) and X_n (inverting X terminal). The X_p and X_n terminal currents are reflected to the respective Z terminals, namely Z_p and Z_n. (It is worth emphasizing that, for this device, there is no direct relation between the Z_p and Z_n terminal currents). The terminal relationship of the DXCCII shown in Figure 2.5 can be characterized with the following equations:

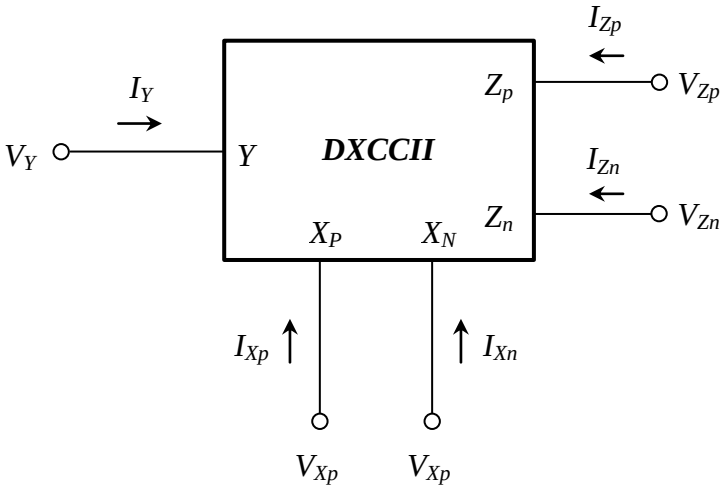


Fig. 2.5. The symbol of the DXCCII.

$$V_{X_P} = \beta_1 V_Y, V_{X_n} = -\beta_2 V_Y, I_Y = 0, I_{Zn} = \alpha_n I_{Xn}, I_{Z_P} = \alpha_P I_{X_P}, \quad (4)$$

Where ideally $\beta 1 = \beta 2 = 1, \alpha_n = \alpha_p = 1$ and they represent the voltage or current transfer ratios of the DXCCII.

The CMOS realization of the classical DXCCII is shown in Figure 2.6 (H.A Alzaher et al, 2000, G. Ferri et al, 2003). The Z_n output resistance of the DXCCII can be found as

$$R_{Zn} = (r_{ds14}) // (r_{ds20}) \quad (5)$$

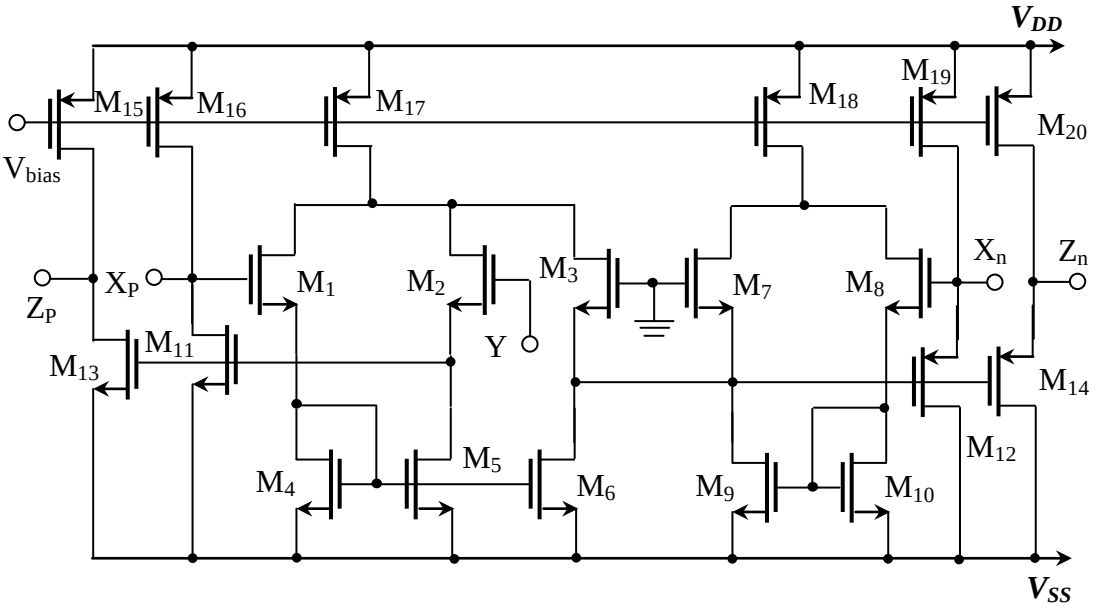


Fig. 2.6. Classical dual-X second generation current conveyor (F. Kacar et al, 2010).

The classical DXCCII is expected to have a suitable current and voltage transfer accuracy in most of its applications. However the output resistance of DXCCII can further be improved to fairly reasonable level to enable easy cascading of DXCCII based circuits in current-mode operation. To increase the output resistance a new DXCCII based on using improved active-feedback cascode current mirror (IAFCCM) (F. Kacar et al, 2010) in the output stages of the conveyor is proposed. The proposed high performance DXCCII is shown in Figure 2.7. A major advantage of IAFCCM circuit is that the output conductance and the feedback capacitance are 100 times lower than the standard current mirror circuit (F. Kacar et al, 2010). Although the number of transistors used in the structure of the proposed DXCCII is larger than the classical one, the output resistance of this DXCCII is much higher. From the Figure 2.7, the output resistance at terminal Z of the proposed high performance DXCCII can be calculated as

$$R_{Zn} = \left[g_{m24} g_{m22} r_{ds23} r_{ds32} \left(r_{ds22} \,//\, r_{ds20}\right)\right] // \left[g_{m32} g_{m30} r_{ds31} r_{ds32} \left(r_{ds30} \,//\, r_{ds28}\right)\right] \quad (6)$$

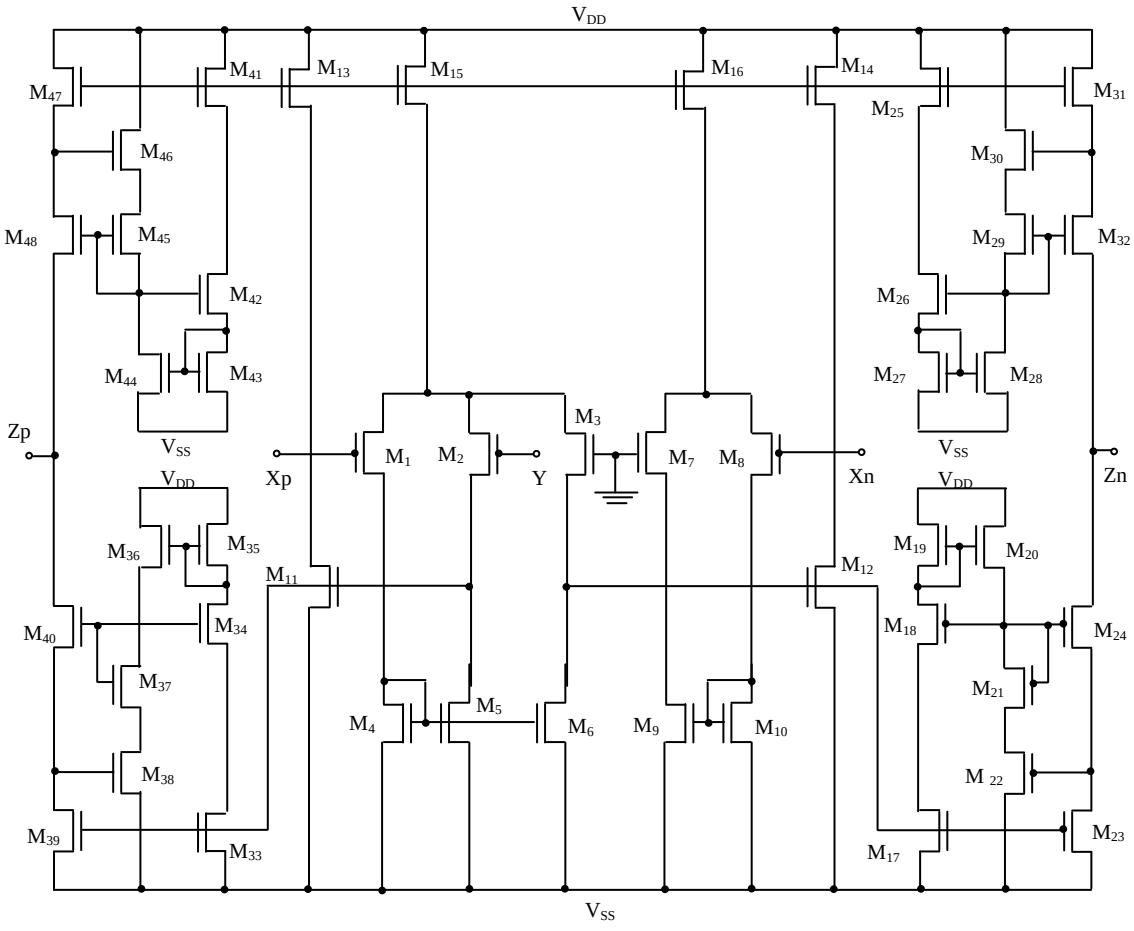


Fig. 2.7. The high performance dual-X second generation conveyor (F. Kacar et al, 2010).

2.2.3. Reza Chavoshisani DCCII, 2011

Equation (7)-(9) and Figure 2.8, demonstrate differential second generation current conveyor (DCCII) block and matrix characteristic, respectively (M. Fakhfakh et al, 2010). Also, matrix characteristic results are shown as following equations:

$$I_{Z1} = I_{X1} - I_{X2} \tag{7}$$

$$I_{Z2} = I_{X2} - I_{X1} \tag{8}$$

$$V_{X1} = V_{X2} = V_Y \tag{9}$$

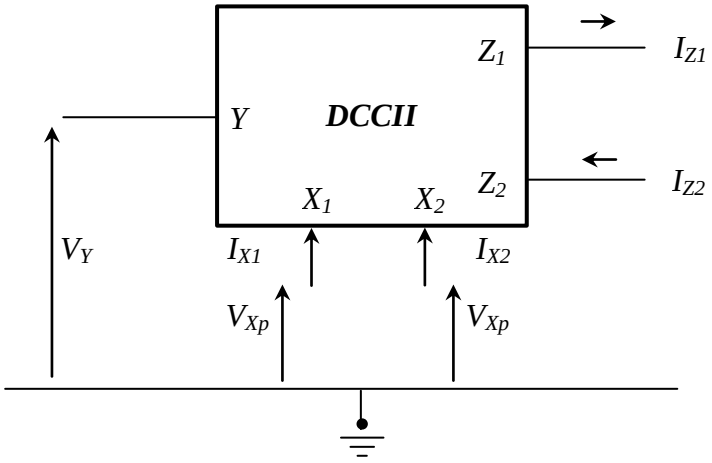


Fig. 2.8. DCCII Block representation.

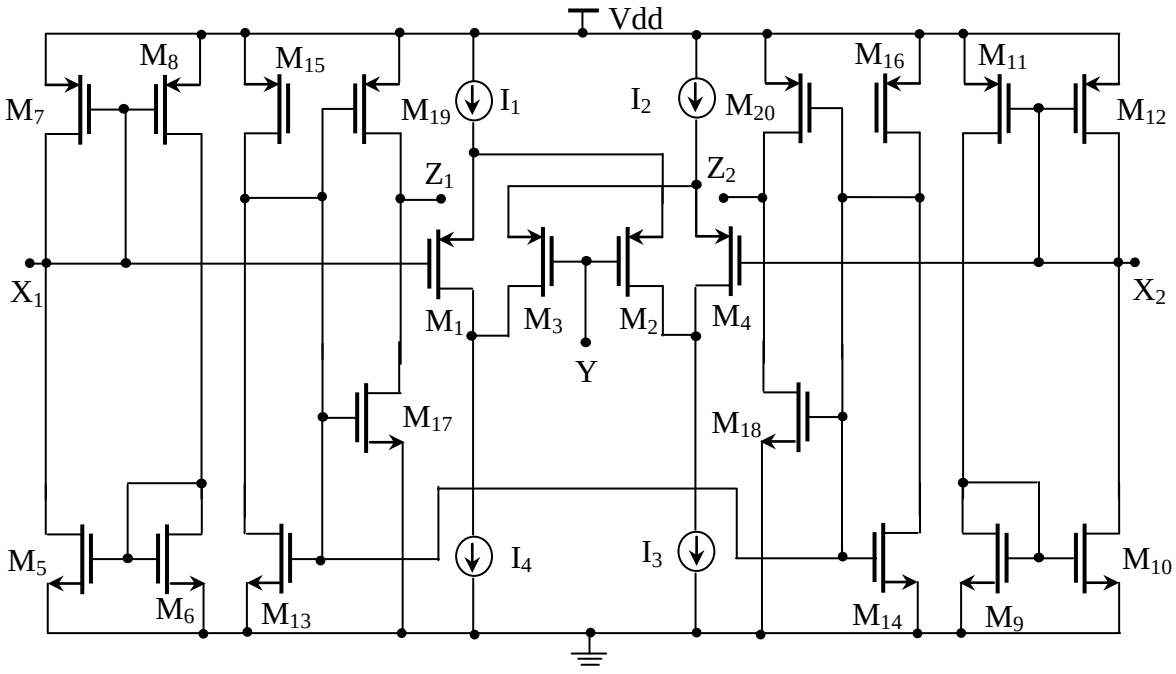


Fig. 2.9. Complete schematic of DCC-CCII (R. Chavoshisani et al, 2011).

Neglecting the mismatch effect of M_1–M_4 transistors could lead to equal gate-source voltages. As a case in this point, the unity voltage transfer function (V_X/V_Y, Equation (9)) is ensured by using differential pair transistors M_1–M_4. Furthermore, for calculating the X terminal parasitic impedance common small signal model are used. Equation (10) and (11) are the exact and approximate amount of input impedance, respectively. Practically, bias conditions make the transconductance value is about 500 μV/A and hence a 2 KΩ input impedance. The mentioned transconductance is justified by M_7–M_8 and M_{11}–M_{12} transistors. In addition, to obtain equal output impedances and full swing in low current two inverters are added to the Z terminals.

$$R_X = \frac{1}{g_{m7}} \| r_{07} \| r_{05} \tag{10}$$

$$R_X \cong \frac{1}{g_{m7}} \tag{11}$$

2.2.4. BJT-DCCII Implementation, Metin DCCII, 2012

DCCII (Elwan and Soliman 1996; Ciftcioglu, Kuntman, and Zeki 2004) is a five-port analogue building block. Considering the non-idealities caused by the physical implementation of the DCCII, it is described with a matrix equation as follows

$$\begin{bmatrix} V_{XN} \\ V_{XP} \\ I_{Z+} \\ I_{Z-} \\ I_Y \end{bmatrix} = \begin{bmatrix} 0 & 0 & \beta_1 \\ 0 & 0 & \beta_2 \\ \alpha_P & -\alpha_N & 0 \\ \alpha_N & -\alpha_P & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{XP} \\ I_{XN} \\ V_Y \end{bmatrix} \tag{10}$$

Where ideally $\beta_1=\beta_2=1$ and $\alpha_N=\alpha_P=1$ represent the voltage and current transfer ratios of the DCCII, respectively. All current directions are flowing towards the terminals, as shown in Figure 2.10.

The proposed BJT–DCCII implementation is shown in the Figure 2.10. Transistors Q_1–Q_6 realise mixed translinear loops (A. Fabre 1983) by transferring Y-terminal potential to both X_N and X_P terminals. The current source I_0 and transistors Q_7–Q_{15} provide biasing for the mixed translinear loops. The transistors Q_{16}–Q_{27} form a current differencing circuit at the Z-terminals from the currents flowing in to the X_N and X_P terminals.

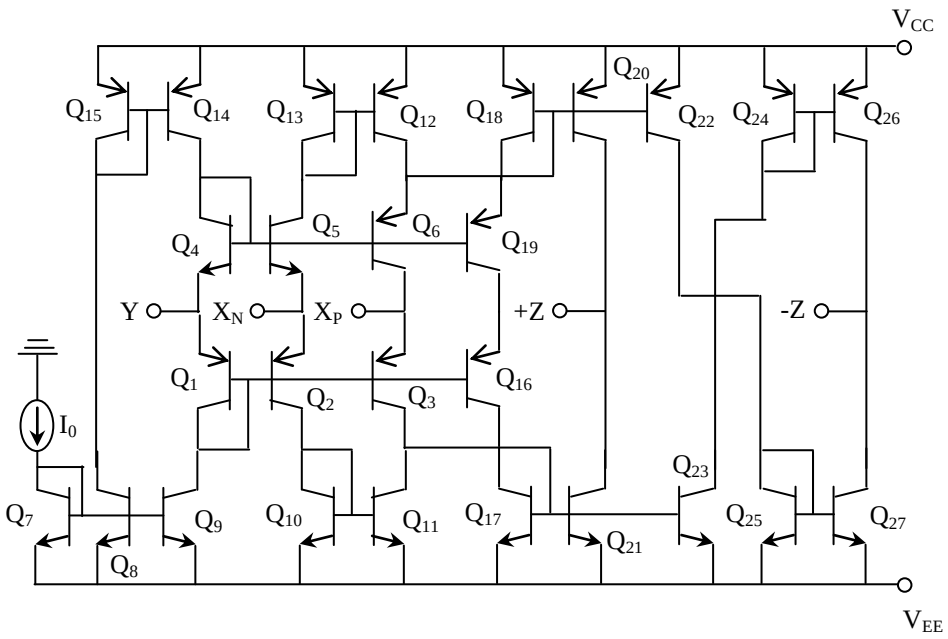


Fig. 2.10. The introduced BJT second generation differential current conveyor (DCCII) (B. Metin et al, 2012).

2.2.5. Bilgin Metin DCCII, 2014

The DCCII is a five-terminal analog building block, whose circuit symbol is shown in the Figure 2.11. The difference of the currents at the X_P and X_N terminals is reflected to the Z terminals. The voltage potential of the Y terminal is copied to the X_P and X_N terminals. Considering the non-idealities caused by the physical implementation of the DCCII, it is described with the following hybrid matrix:

$$\begin{bmatrix} V_{XN} \\ V_{XP} \\ I_{Z+} \\ I_{Z-} \\ I_Y \end{bmatrix} = \begin{bmatrix} 0 & 0 & \beta_1 \\ 0 & 0 & \beta_2 \\ \alpha_P & -\alpha_N & 0 \\ \alpha_N & -\alpha_P & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{XP} \\ I_{XN} \\ V_Y \end{bmatrix} \tag{11}$$

where β_i and α_i for i=N,P represent the voltage and current gains of the DCCII that are ideally equal to unity.

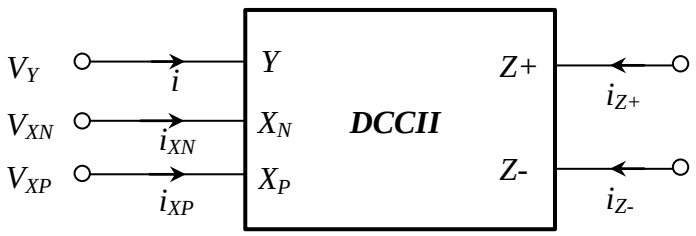


Fig. 2.11. Circuit symbol of the DCCII.

Unlike DCCII design that includes 21 transistors in H.O. Elwan et al, 1996, the DCCII in S. Ciftcioglu et al, 2005 uses 34 transistors. However, it has very high output impedance due to active feed-back cascade current mirrors. In Figure 2.12, as explained in S. Ciftcioglu et al, 2005, the input currents i_{XN} and i_{XP} are applied to the drain of transistors M_{12} and M_{14}, respectively. The Y terminal voltage is applied to the gate of transistors M_2 and M_5. Because M_1, M_2, M_5, and M_6 are matched transistors; the voltage at Y terminal is conveyed to the terminals X_N and X_P. The difference between the X_P and X_N currents is conveyed to the Z terminals by the mirroring action of transistors M_{15}–M_{18} and M_{19}–M_{22}. Transistors M_{23}–M_{34} form the accurate active-feedback CMOS cascode current mirrors of the output stages.

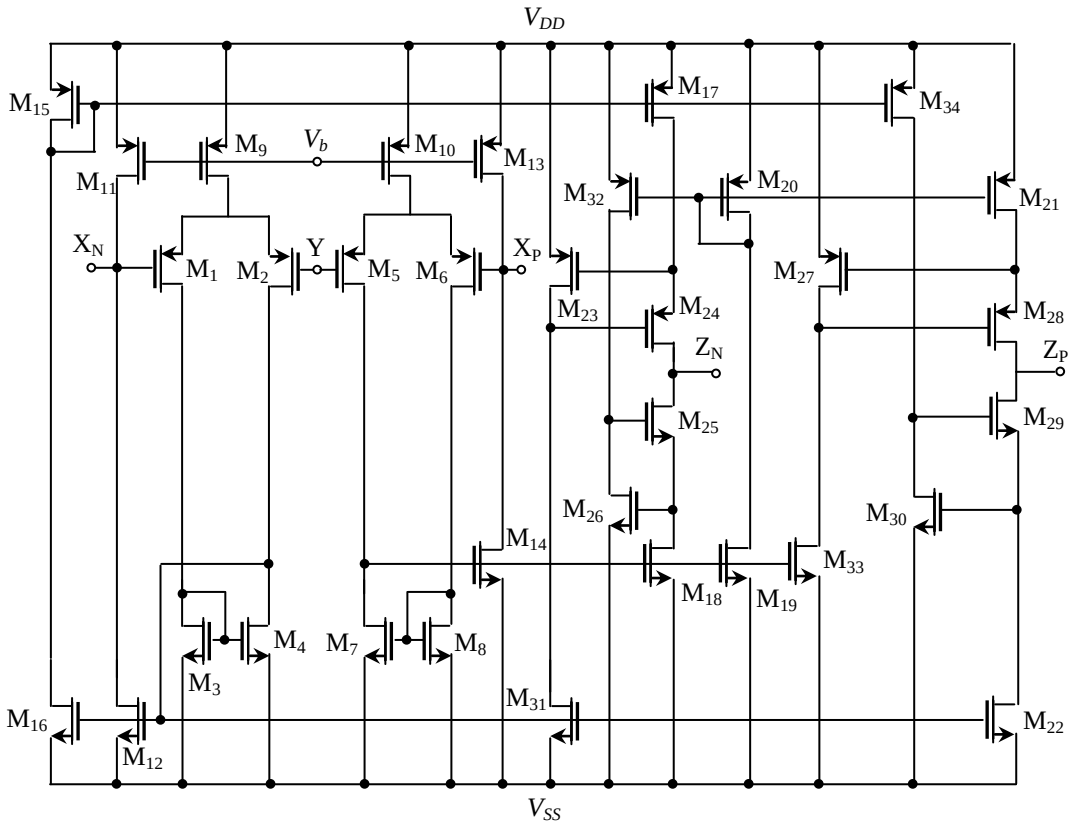


Fig. 2.12. A CMOS implementation of the DCCII (B. Metin et al, 2014).

2.2.6. Emre Arslan DCCII, 2016

The developed internal structure consists of a class AB input stage based on high performance translinear loop, where one is a CS stage, and the other is current mirror stage. Compared to the previously published CMOS DCCII implementations (H.O. Elwan et al, 1996, S. Ciftcioglu et al, 2005, B. Metin et al, 2012a, B. Metin et al, 2012b), here proposed circuit has very low equivalent input impedances at both

input X_n and X_p ports and high equivalent impedance at the output port Z due to the used source followers with local feedback.

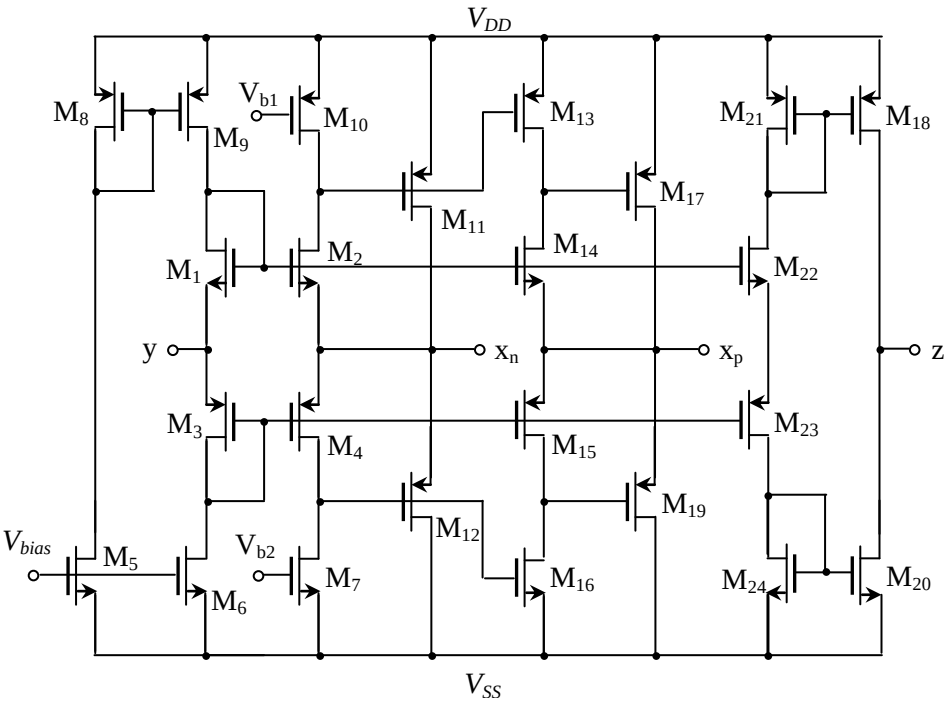


Fig. 2.13. The proposed high performance CMOS DCCII (E. Arslan et al, 2016).

The novel CMOS structure of the proposed DCCII, which is given in the Figure 2.13, is based on class AB translinear loop input stage formed by transistors M_1–M_4, while CS and current mirror stages are consist of transistors M_{11}–M_{17}, M_{19}, and M_{18}, M_{20}–M_{24}, respectively. Transistors M_6, M_7 and M_9, M_{10} have equal currents and both pairs serve as DC current sources for the translinear loop. Transistor pair M_2 and M_{11} forms the source follower with local feedback so-called super source follower (SSF) to obtain very small equivalent resistance at port X_n with other SSF pair M_4 and M_{12}. Other SSF pairs of transistors M_{14}, M_{17} and M_{15}, M_{19} are used to obtain very small equivalent resistance at port X_p. Current mirror pairs M_{21}, M_{18} and M_{24}, M_{20} are used to obtain the difference current at output port Z.

The equivalent resistance seen on port y of class AB input stage is equal to

$$R_Y = \left(\frac{1}{g_{m1}} + r_{09}\right) \left\| \left(\frac{1}{g_{m1}} + r_{06}\right)\right. \tag{12}$$

where g_{mk} and r_{ok} are transconductance and output resistance of k-th MOS transistor, respectively. The equivalent resistance seen on ports x_n and x_p are equal to (E. Arslan et al, 2013):

$$R_{xn} = \frac{1}{g_{m11}\left(1+g_{m2}r_{02}\right)} \Big\| \frac{1}{g_{m12}\left(1+g_{m4}r_{04}\right)} \tag{13}$$

$$R_{xp} = \frac{1}{g_{m17}\left(1+g_{m14}r_{014}\right)} \Big\| \frac{1}{g_{m19}\left(1+g_{m15}r_{015}\right)} \tag{14}$$

Finally, the equivalent resistance seen on port z can be calculated simply as

$$R_z \cong \frac{r_{18}r_{20}}{r_{18}+r_{20}} \tag{15}$$

hence, from output resistance of transistors M_{18} and M_{20}.

2.2.7. Sajjad Shahsavari DCCII, 2015

Proposed technique requires a DCCII block. A typical differential current conveyor that uses two second generation current conveyors depicted in Figure 2.14 (G. Ferri et al, 2003, A. Smith et al, 1970, H.B Gabbouj et al, 2008). As illustrated in Figure 2.14, two CCII form a DCCII where their Y terminals connect to each other and X terminals are triggered with input current source. Also, Z terminals are connected with subtractor input terminals. Current subtractor subtracts out-put currents of each CCII, $I_{out}=I_{+}-I_{-}$. Figure 2.15 shows the circuit of a second generation current conveyor.

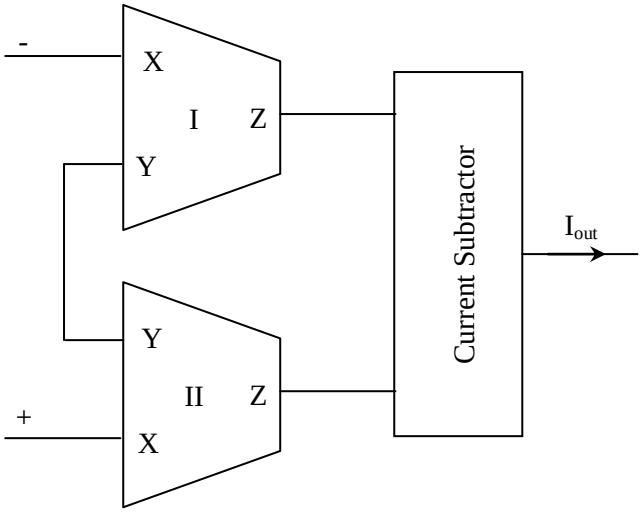


Fig. 2.14. A Block diagram of differential current conveyor.

This type of current conveyor describe by a matrix which is pointed in Equation (16).

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \tag{16}$$

From above matrix, it is obvious that *X* terminal is low impedance node, *Y* and *Z* terminals are high impedance nodes. Current of *Z* terminal is equal to *X* terminal. By employing second generation current conveyor, both inputs of DCCII are low impedance nodes that do not cause low frequency poles.

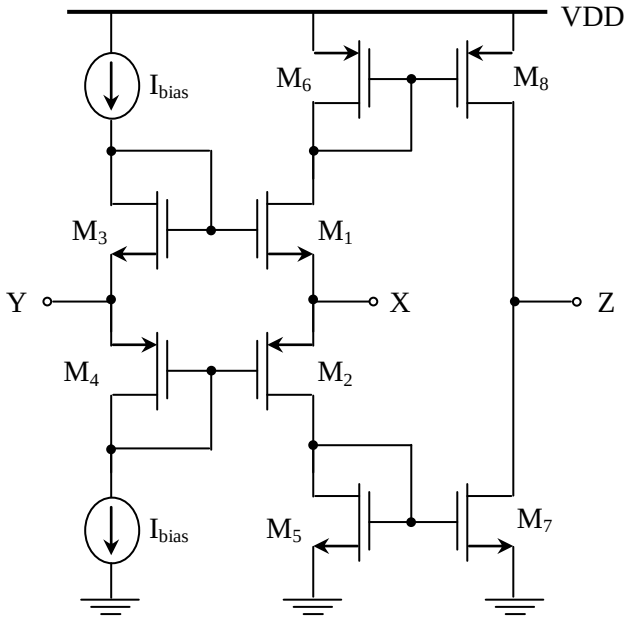


Fig. 2.15. Circuit of second generation current conveyor (G. Ferri et al, 2003).

2.2.8. Montree Kumngern DCCII 2014

The symbol of DCCII is shown in Figure 2.16. The ideal DCCII can be characterized as

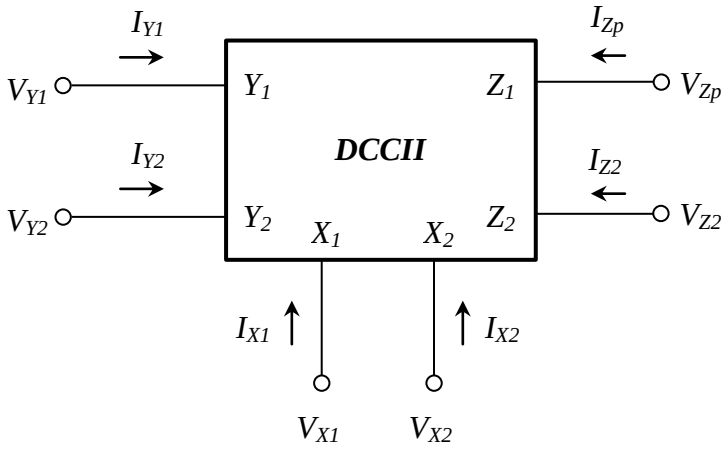


Fig. 2.16. Circuit Symbol of DCCII.

$$\begin{bmatrix} V_{X1} \\ V_{X2} \\ I_{Z1} \\ I_{Z2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & -1 \\ 0 & 0 & -1 & 1 \\ 1 & -1 & 0 & 0 \\ -1 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{X1} \\ I_{X2} \\ V_{X1} \\ V_{X2} \end{bmatrix} \quad (17)$$

Ideally, the terminals Y_1, Y_2, Z_p and Z_n possess high impedance level where as the terminals X_p and X_n possess low impedance level for DCCII. Figure 2.17 shows a new low-voltage (LV) low-power (LP) DCCII using bulk-driven and quasi-floating-gate techniques. The differential input stages are consisted of three differential amplifiers. Each differential amplifier uses the BD-QFG MOS transistor technique (F. Khateb et al, 2013). The operation of a BD-QFG MOS transistor can be explained by M_1, M_{b2}, and C_1. M_{b1} is operated as cut-off region to create a large resistance value. The input signal will excite via C_1 to the quasi-floating gate from one side and directly couple to the bulk terminal from the other side. The BD-QFG-MOS transconductance is given as $g_{m,BD\text{-}QFG}=g_{mb}+g_{m,QFG}$ (F. Khateb et al, 2013). Hence, the transconductance of BD-QFG-MOS transistor is higher than the BD MOS transistor. The minimum needed power supply voltage can be given by $V_{DD(min)}=V_{GS(M7,M8,M9)}+V_{DS\ (M10,M11,M12)}$. The transistors M_1 to M_6 will operate as weak inversion if the voltages V_{GS} are less than their threshold voltages. Transistors M_{19}, M_{20}, M_{21}, M_{10}, M_{11}, M_{12}, M_{28} and M_{29} act as a multiple output current mirror for applying the constant current source I_B to each branch of the circuit. The power consumption of the proposed circuit can be obtained appropriately by setting the biasing current I_B. Transistors M_{10}, M_{11} and M_{12} are common for all differential input stages and they form the active load for them. Transistors M_7, M_8 and M_9 act as tail current sources for all differential input stages. The second stage of three differential input stages is created by cascode transistors M_{14}, M_{16}, M_{18}, M_{21} and M_{22}, M_{24}, M_{26}, M_{28}. The cascode transistors are used to ensure that the unity gain connection between the outputs of the second stage x_1 and x_2 terminals ($V_{y1\text{-}Vy2}=V_{x1\text{-}Vx2}$) can be achieved. On the other hand, the cascode transistors M_{13}, M_{15}, M_{17}, M_{20} and M_{23}, M_{25}, M_{27}, M_{29} create the output stage for BD-QFG DCCII at the outputs and they provide the current copies of the X_1 terminal to the Z_1 terminal and the X_2 terminal to the Z_2 terminal.

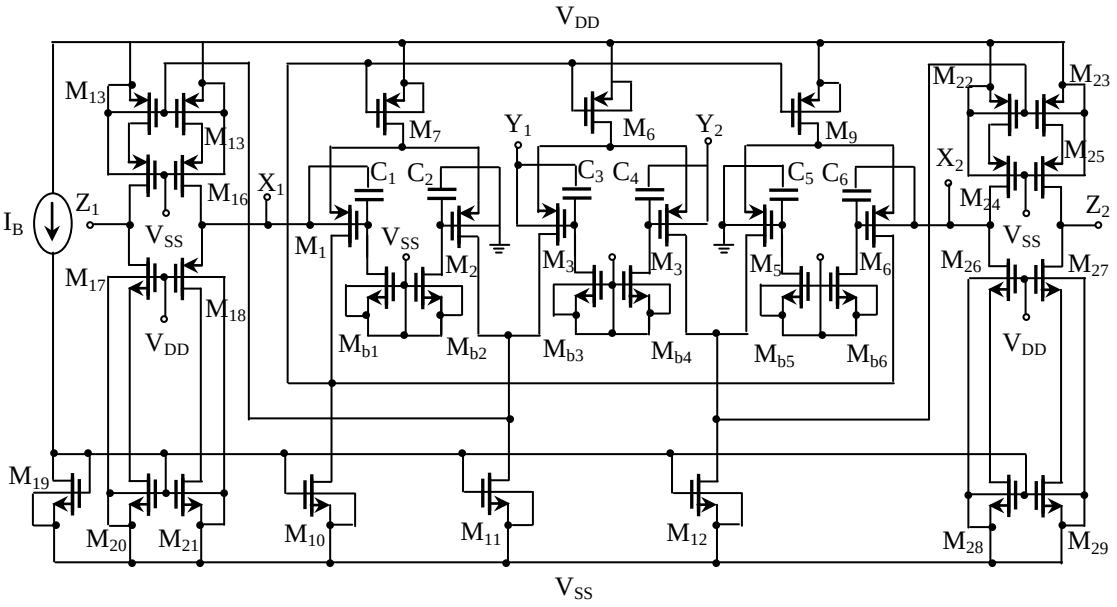


Fig. 2.17. Proposed BD-QFG DCCII (M. Kumngern and F. Khateb 2014).

2.2.9. Sinem Ciftcioglu DCCII 2005

The differential current conveyor is a four-terminal analog building block as shown in Figure 2.18. Describing matrix of the DCCII is given in equation (1).

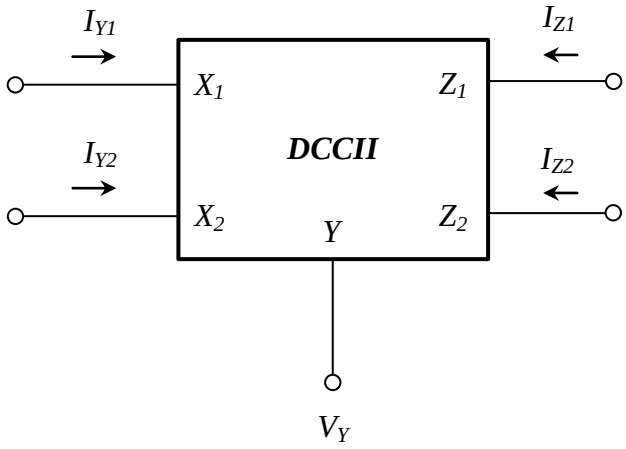


Fig. 2.18. DCCII Symbol.

The MOS realization of the DCCII is shown in Figure 2.19. All transistors are assumed to be operating in the saturation region.

$$\begin{bmatrix} V_{X1} \\ V_{X2} \\ I_{Z1} \\ I_{Z2} \\ I_Y \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 \\ 1 & -1 & 0 & 0 & 0 \\ -1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{X1} \\ I_{X2} \\ V_{Z1} \\ V_{Z2} \\ V_Y \end{bmatrix} \quad (18)$$

As shown in the Figure 2.19, the input currents I_{X1} and I_{X2} are applied to the drain of transistors M_{12} and M_{14}, respectively. The Y terminal voltage is applied to the gate of transistors M_2 and M_5. As M_1, M_2, M_5 and M_6 are matched transistors, the voltage at Y terminal is conveyed to the terminals X_1 and X_2. The difference between the X_1 and X_2 currents is conveyed to the Z terminals by the mirroring action of transistors M_{15}-M_{18} and M_{19}-M_{22}.

M_{23}-M_{34} transistors form the accurate active-feedback CMOS cascode current mirrors of the output stages. Active-feedback CMOS cascode current mirrors have very accurate current reflection ratio, while achieving high output impedance. Thus they can be used in high precision analogue integrated circuits, especially in structures where current mode techniques are used (A. Zeki et al, 1998).

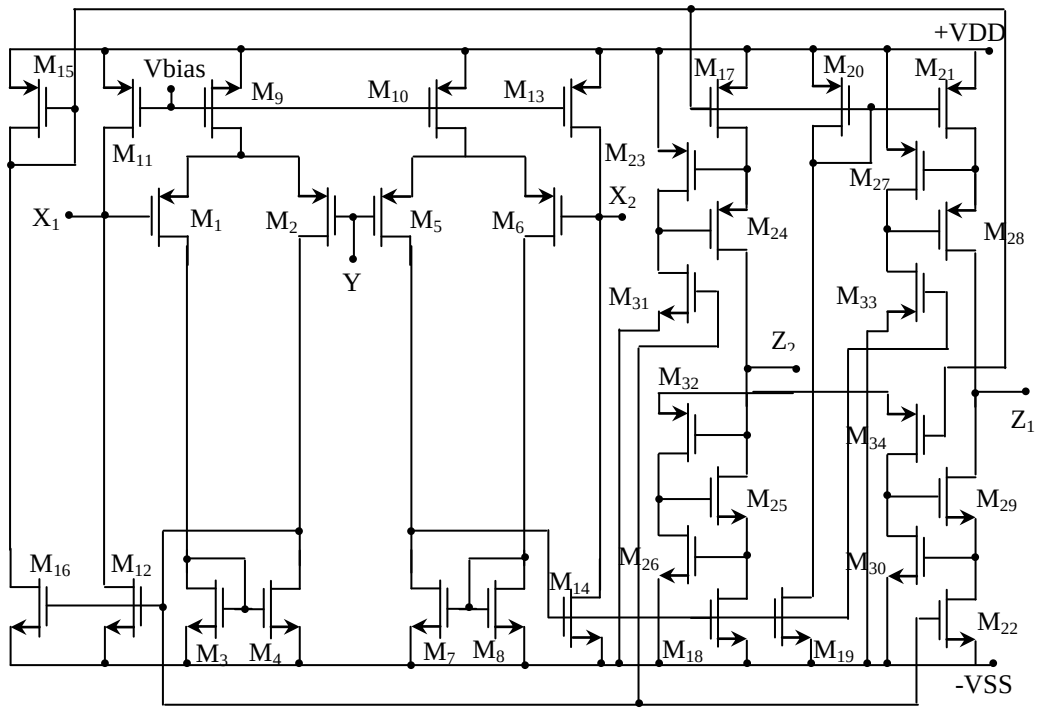


Fig. 2.19. Proposed CMOS DCCII Realization (S. Ciftcioglu et al, 2005).

2.2.10. Hesham F. Hamed DCCII 2001

The differential current conveyor (DCCII) is an analog building block consists of three input terminals (X_l, X_2 and Y) and two output terminals (Z_1 and Z_2). It can be described by the following matrix:

$$\begin{bmatrix} V_{X1} \\ V_{X2} \\ I_{Z1} \\ I_{Z2} \\ I_Y \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 \\ 1 & -1 & 0 & 0 & 0 \\ -1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{X1} \\ I_{X2} \\ V_{Z1} \\ V_{Z2} \\ V_Y \end{bmatrix} \tag{19}$$

The MOS realization of the DCCII is shown in Figure 2.20. All transistors are assumed to be operating in the saturation region with their sources connected to their substrate.

As shown in the Figure 2.20, the input current (I_{x1}) is applied to the drain of the transistor M_3 and the current (I_{x2}) can be applied to the drain of the transistor M_{33}. The current mirror of the transistors Q_1 with Q_2 and Q_{22} are connected to convey the voltage at port (Y) to the terminals (X_l) and (X_2).

A level shifter is connected to improve the input current swing. It is composed of two transistors Q_4 and M_5 for the input current (I_{Xl}), and Q_{44} and M_{55} for the input current (I_{x2}). The current mirror, that composes of M_5 and M_6, conveys the input current (I_{x1}) to the output terminal, and in the same way the input current (I_{x2}) is conveyed by the current mirror that consists of M_{55} and M_{66}.

Transistors M_{11} and M_{12} compose a current mirror and are connected to have an output current opposite to the input current (I_{x1}). The current mirror of M_{111} and M_{112} is connected to have an output current opposite to the input current (I_{x2}). Finally the conveyed currents can be subtracted by connecting the current mirror of transistors M_{57}, M_{56}. The output current is as follows:

$$I_{out1} = I_{M6} - I_{M66} \tag{20}$$

$$= \left(I_{x1}^{+}\right) - \left(I_{x2}^{+}\right) \tag{21}$$

In the same way, an opposite output current can be obtained from the current mirror of transistors M_{15} and M_{16}. The output current will be as follows:

$$I_{out2} = I_{M12} - I_{M112} \tag{22}$$

$$= \left(I_{x1}^{-}\right) - \left(I_{x2}^{-}\right) \tag{23}$$

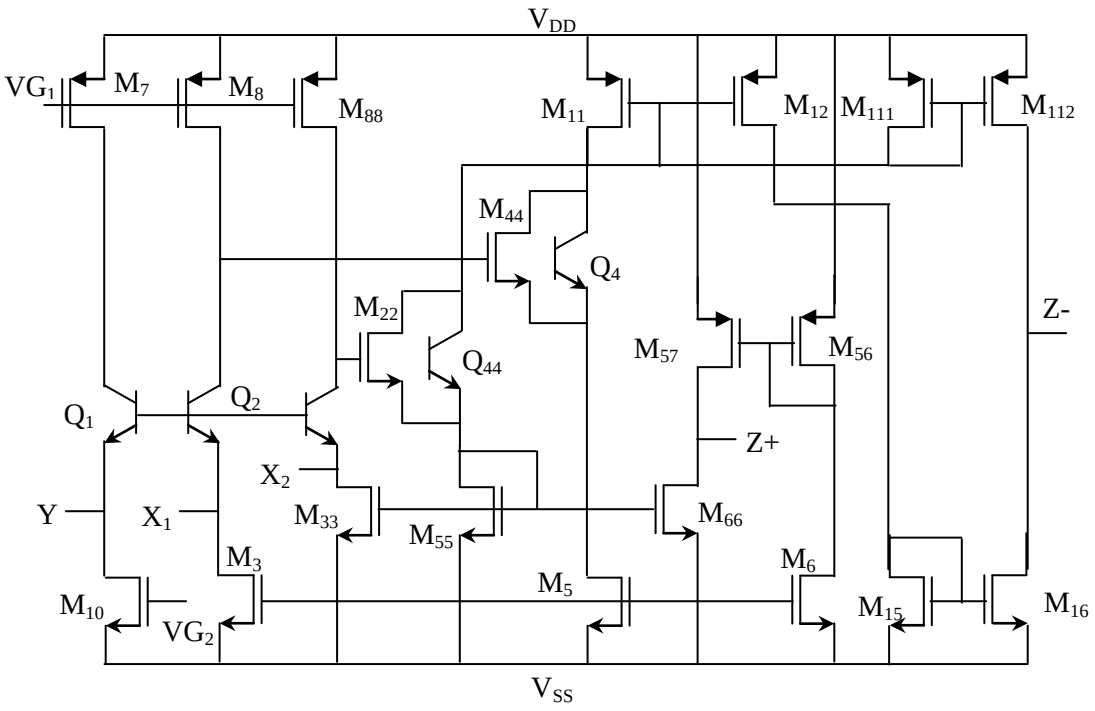


Fig. 2.20. The differential current conveyor (H.F. Hamed et al, 2001).

2.3. DCCII Implementation Using AD844AN

The second generation differential current conveyor can also be implemented using the commercially available IC called a current feedback operational amplifier (CFOA) AD844AN (Y. K. Lo et al, 2007, Y. K. Lo et al, 2007, Y. K. Lo et al, 2006, R. Pandey et al, 2011). The CFOA is a three terminal active device. The circuit symbol of the CFOA is shown in the Figure 2.21 (AD844 Data sheet). The DCCII implementation using the IC AD844AN is shown in the Figure 2.22. Two AD844AN ICs are used to construct the DCCII.

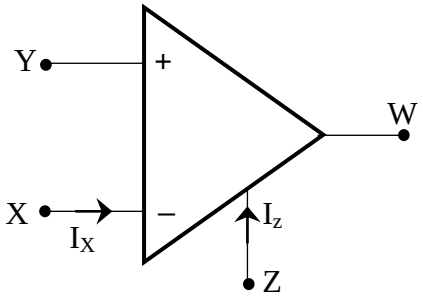


Fig. 2.21. CFOA (AD844AN) circuit symbol.

The DCCII don't contain any voltage buffer. Therefore, connecting W terminal of CFOA1 to "-" of CFOA2 (instead of Z to "–" as it is in the proposed designs) realizes different from proposed circuits. In other words, in the above mentioned case simulated and realized circuits are not identical. Using the buffer of CFOA2 will not modify the mathematical model of the proposed circuits and will have positive effect as the circuits are able to design fully cascadable applications.

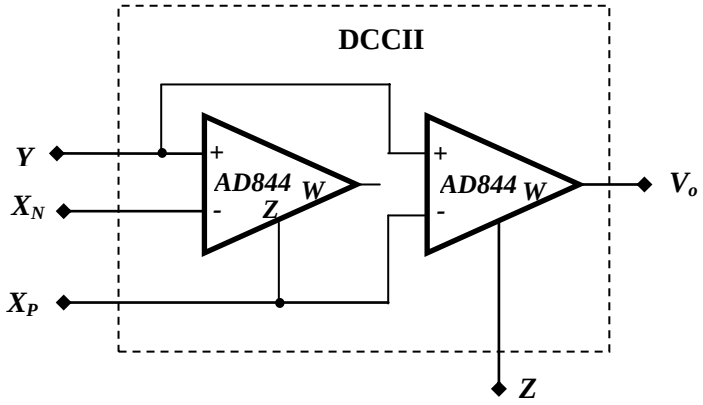


Fig. 2.22. Experimental setup of DCCII using AD844AN.

Here in this context it should be noted that the output circuitry of CFOA is voltage buffer. Hence, by using the full potential of the CFOA2, the proposed circuits have both high-input and low-output impedances, simultaneously.

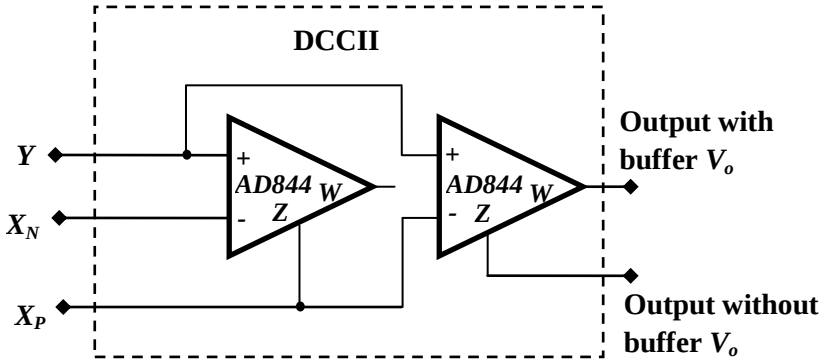


Fig. 2.23. The hardware prototype model of DCCII incorporated using AD844AN.

With the schematics shown in Figures 2.22 and 2.23, the proposed circuits in chapter 4 can be implemented on the laboratory bread board to check the theoretical analysis.

2.4. Summary

The evaluation of the current mode devices and in particular the existence of the DCCII for the implementation of various applications are discussed and presented in this chapter. Considering the vital features of the DCCII many researchers introduced various configurations of the DCCII with the existed methodologies. Among all these devices the common and differencing features are explained and the main CMOS realization of the active element is depicted with the relevant information.

CHAPTER III

REVIEW OF LITERATURE

3.1. Introduction

In addition to above listed ABBs, the differential current conveyor (DCCII) was introduced in 1996 (H.O. Elwan et al, 1996) as the first current-mode active element with current differencing capability. However, in the literature it has not received as much as attention than the conventional CDBA presented in 1999 (C. Acar et al, 1999). In fact, the DCCII combines the simplicity of the classical CCII (A. Sedra et al, 1970) with current differencing feature of the CDBA. Therefore, the DCCII looks like a CDBA for current differencing operation, but it has an additional voltage terminal like CCII, which has high-input impedance and can be useful for cascading VM circuits. In addition, the DCCII includes fewer numbers of transistors than CDBA, which has a supplementary voltage buffer stage.

3.2. DCCII Applications

New CMOS realization of high performance differential current conveyor (DCCII) is presented. Presented high performance differential current conveyor is a useful analog building block with the advantage of wide bandwidth. It can be directly used with MOS transistors operating in the ohmic region to implement some essential analog functions. In this study, to increase the variety of DCCII circuits in the literature, its novel implementations using different configurations of DCCII are presented. DCCII is used for realizing many applications viz. Filters, Oscillators, Sine Wave Generators, Square Wave Generators, Current Comparators, Inductance Simulators, Multipliers, Frequency dependent negative resistance (FDNR), Frequency Compensation Circuits.

3.3. All-pass Filters Using DCCII

In the existed literature till now there are three all pass filter circuits are existed and among those three, two circuits are realized using voltage mode approach and the third one is realized in current mode approach. The all-pass filter circuit using single DCCII, two resistors and a single capacitor is shown in Figure 3.1 (B. Metin et al, 2012).

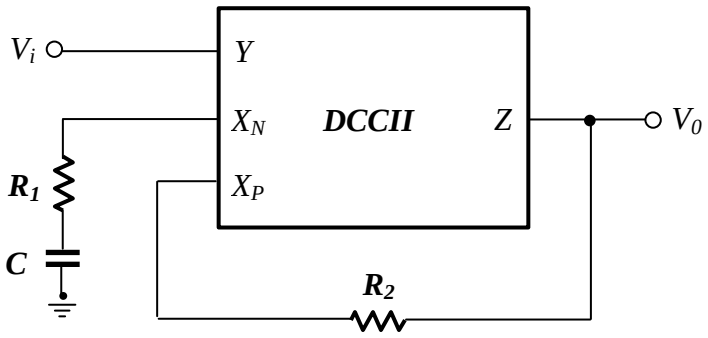


Fig. 3.1. The first-order all-pass filter employing a DCCII (B. Metin et al, 2012).

Its voltage transfer function can be expressed as:

$$\frac{V_0}{V_i} = \frac{2 + 2sCR_1 - sCR_2}{2 + 2sCR_1} \tag{1}$$

Here it should be emphasized that the presented circuit has resistors in series to its X terminals. Hence, by selecting sufficiently high values of R_1 and R_2 the unwanted effects of the parasitic resistors at the X terminals to the operation and resistor matching condition of the circuit can be easily compensated. The simulation shows that the current gain of the DCCII a bit alters from α_P while the voltage gains β_N and β_P are equal. The f_{-3dB} frequency of voltage transfers is significantly higher than cut-off frequency of the current transfers. The equivalent input and output noises at are found as 43.29 and 39.37 $nv/\sqrt{Hz}$, respectively. This circuit has the inconsistencies in magnitude and phase because of non-idealities existed.

The current mode as well as voltage mode all-pass filter circuits using single DCCII, two resistors and a single capacitor is shown in Figures 3.2 and 3.3 (Emre Arslan et al, 2016). A novel translinear loop based, high performance Complementary Metal-Oxide-Semiconductor (CMOS) second-generation differential current conveyor (DCCII) is introduced. By using super source follower transistors, very low equivalent impedances are obtained at input terminals X_N and X_P. In addition, new voltage-mode (VM) and current-mode (CM) first-order all-pass filters (APFs) are proposed to highlight the performance of the designed CMOS DCCII.

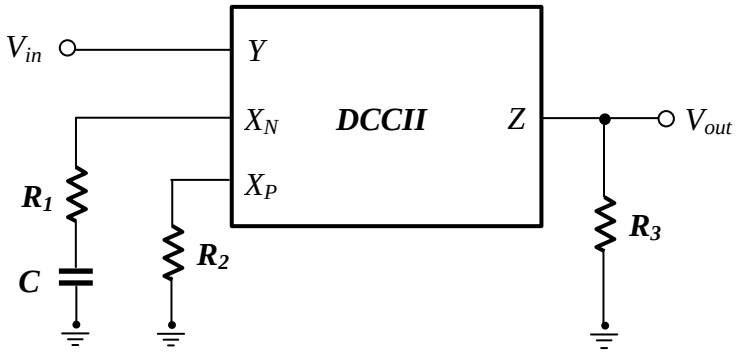


Fig. 3.2. First-order voltage-mode AP filter.

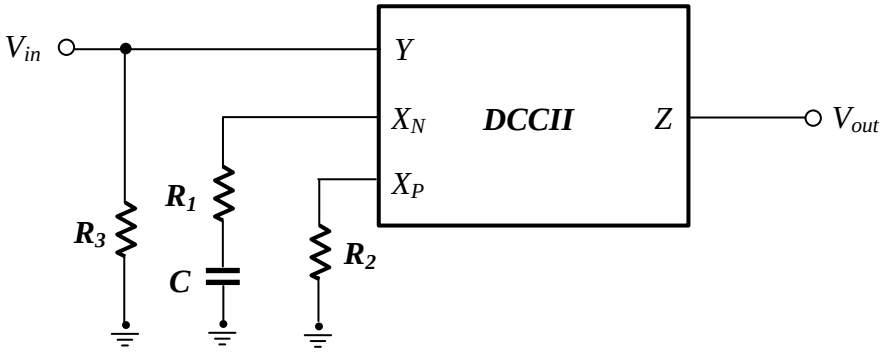


Fig. 3.3. First-order current-mode AP filter.

$$T_{VM}(S) = \frac{V_{out}}{V_{in}} = -\frac{sCR-1}{sCR+1} \tag{2}$$

$$T_{CM}(S) = \frac{I_{out}}{I_{in}} = \frac{sCR-1}{sCR+1} \tag{3}$$

Hence, their sensitivities to passive elements are unity in relative amplitude. The proposed VM APF in Figure 3.2 has high input impedance and CM circuit in Figure 3.3 has high output impedance. Hence, both proposed APFs have the advantage of being cascadable, i.e. there will be no need for additional voltage buffer or current follower in case of their connection into a voltage or current-mode signal processing channel, respectively.

Note that at high frequencies the deviations in gain and phase characteristics are affected by the poles of voltage and current gains as well as by the external terminal parasitics of the readily available ICs. Moreover, according to datasheets, the

passive element tolerances of selected discrete components are 2% and 5%, which may also affect the precision of f_p.

3.4. DCCII Based Band-Pass Filter

As the applications of the presented DCCII, a mixed mode second order band-pass filter is presented by S. Ciftcioglu et al, 2005.

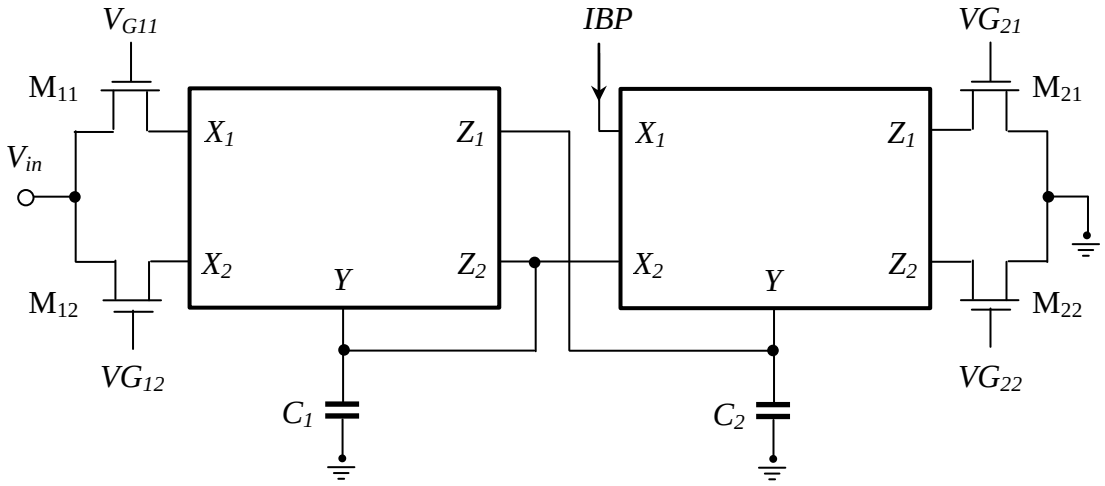


Fig. 3.4. A mixed mode second order band-pass filter.

The circuit shown in Figure 3.4 represents a mixed mode second order band-pass filter based on the DCCII. Transistors M_{11}, M_{12}, M_{21} and M_{22} are operating in the ohmic region with their nonlinearities canceled out as discussed in the next section of 3.8. The input to this filter section is a voltage while the output is a current and the transfer function is given by:

$$\frac{I_{BP}}{V_i} = \frac{s\dfrac{G_1 G_2}{C_2}}{s^2 + S\dfrac{G_1}{C_1} + \dfrac{G_1 G_2}{C_1 C_2}} \tag{4}$$

Where, $$G_1 = K_1\left(V_{G11} - V_{G12}\right) \tag{5}$$

$$G_2 = K_2\left(V_{G21} - V_{G22}\right) \tag{6}$$

It is then shown the properties of the block are suitable for designing current mode circuits using CMOS technology.

3.5. DCCII Based Multiple Output Filter

This proposed filter has a low voltage (±1.5V) low power (800µW) multiple output filter performing low-pass, band-pass, high-pass and all pass functions. The filter has been implemented using improved differential second generation current conveyors (DCCIIs) and MOS resistive circuits (MRC) instead of resistances. Thanks to the improved topology of the DCCIIs, the proposed solution allows both to perform the fully integration in a standard CMOS technology and to have the angular frequency and the quality factor easily tunable with excellent agreement of theoretical behavior. Moreover the proposed filter presents low active and passive component sensitivities.

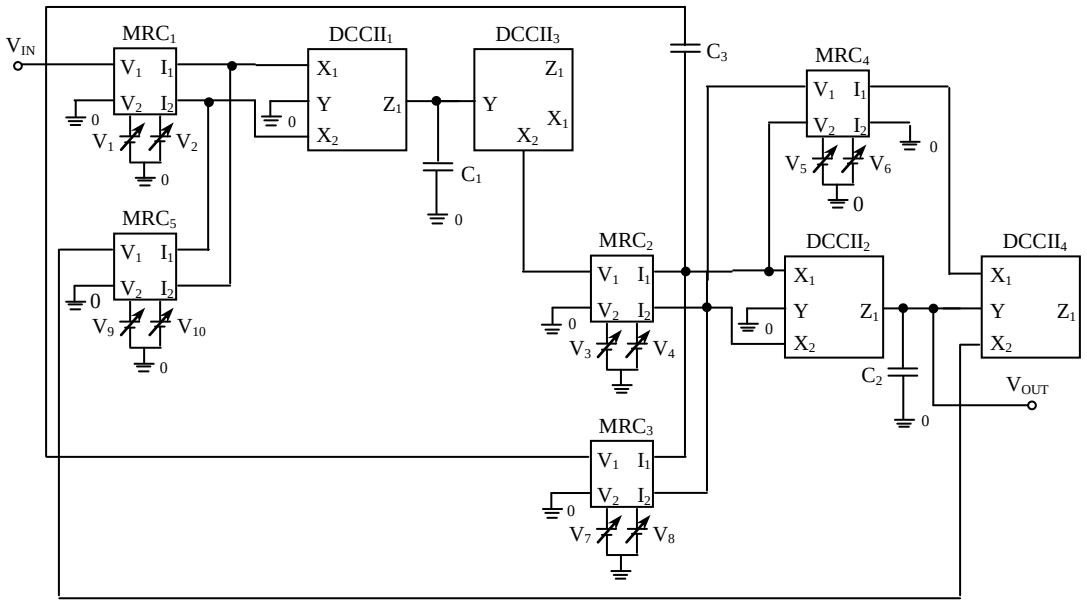


Fig. 3.5. The proposed filter with improved DCCII and MRC.

The proposed second-order multifunction filter is shown in Figure 3.5. Routine analysis of Figure 3.5 circuit gives the following voltage transfer function:

$$\frac{V_0}{V_i} = \frac{s^2\frac{C_3}{C_2} + s\frac{G_3}{C_2} + \frac{G_2G_1}{C_1C_2}}{s^2 + S\frac{G_4}{C_2} + \frac{G_2G_5}{C_1C_2}} \tag{7}$$

Where

$$G_i = \frac{I_{1i} - I_{2i}}{V_{1i} - V_{2i}} \tag{8}$$

Where G_i is the conductance of the i-th MRC. The bi-quadratic transfer function can be obtained considering that the output current of each DCCII depends on the output currents of MRC connected at input nodes, so specialization of the numerator in Equation (7) gives the different suitable transfer functions and filter functionalities.

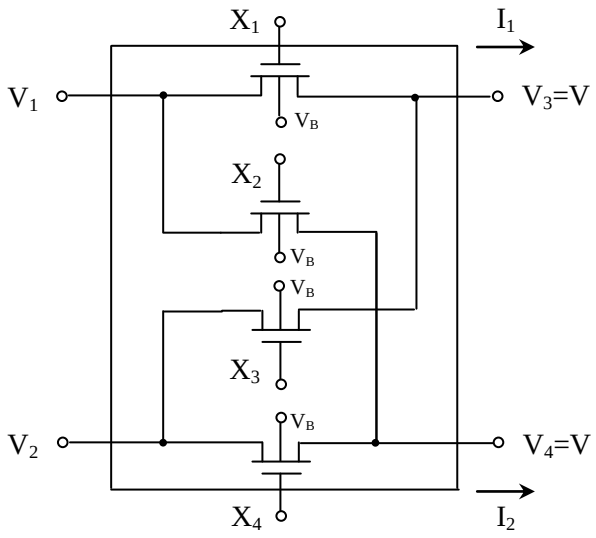


Fig. 3.6. MOS Resistive Circuit.

It does not employ external resistor and Q-factor and angular frequency ω_0 can be tuned electronically by adjusting the conductance of the MRC. These characteristics make this filter very suitable for a complete on chip integration.

3.6. DCCII Based Current Comparator

Comparators are most significant part of analog integrated circuits after operational amplifiers (R. Gregorian et al, 1999, G. Palumbo et al, 1999). Current mode approach advantages lead to current comparator interest in integrated circuit. Differential current conveyor II (DCCII) is designed, modified, and exploited as a comparator with reduced propagation delay and power consumption. New DCCII decreases propagation delay and increases comparator accuracy considerably.

The current comparator concept as expressed by H. Lin et al, 2000 and shown in Figure 3.7 is as follows; the input current is injected into input stage and is converted to the voltage V_{IN} and V_1 by amplifier A_1 and voltage buffer A_2. V_1 is amplified using the high gain amplifier (A_3) to generate the output logic voltage level. A modified DCCII is used as input stage of the new proposed current comparator due

to the low input impedance at current nodes X_1 and X_2, and the inherent current to voltage conversion property of the DCCII circuit.

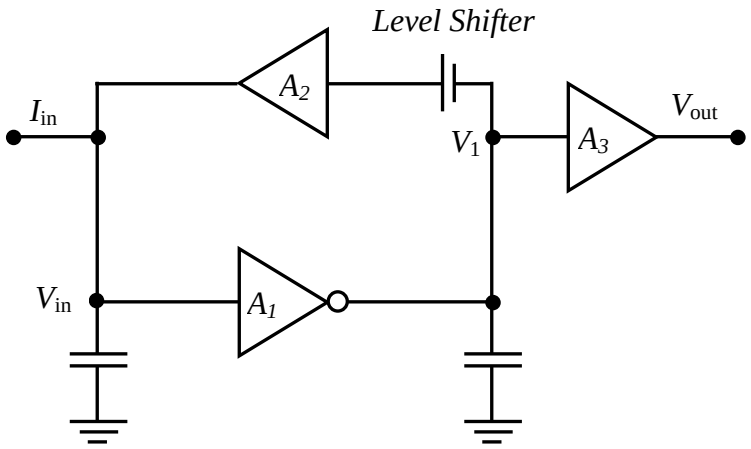


Fig. 3.7. Current comparator concept model.

Due to a two gate stage design, the comparator could operate appropriately in low voltages applications. In addition, circuit could be enhanced by replacing ordinary current mirrors with Wilson current mirror and other alternative and prevalent current mirrors (B. Sedighi et al, 2007, S.J. Azhari et al, 2011, B. Razavi et al, 2001) to obtain accurate current copies and higher output impedances while low voltage operation decrease significantly. Wilson current mirror that function well at all current levels, ranging from weak inversion to strong inversion. Also can operate on a low power-supply voltage of a diode drop plus two saturation voltages and features a wide output-voltage swing with cascode-type incremental output impedance. In order to unify output resistance, two inverters are added at the output stage. Therefore, output parasitic impedances are restricted by $r_o/2$ and boosted by enlarged transistor's length.

3.7. DCCII Based Inductance Simulator

In the literature several lossless (pure) synthetic inductance simulators have been proposed since direct physical implementation of inductors on an integrated chip may not satisfy performance requirements of the circuits in comparison to resistors and capacitors in the integrated circuit (IC) realization point of view. For example, they have larger chip area than other passive circuit elements when high inductance values are needed. Therefore, during last few decades the design of synthetic inductors has received considerable attention. The most famous inductance simulators were proposed by Ford and Girling et al, 1966 and A. Antoniou et al, 1969, respectively.

In this study, a differential current conveyor (DCCII) (Elwan and Soliman, 1996) implementation is introduced with two new inductance simulator circuit examples. The proposed circuits enjoy compensating for the effect of the parasitic resistors (R_X) at X-terminals of the DCCII. Like other inductor simulators that include minimum number of elements in literature, the presented circuits require a resistor matching condition. However, the R_X parasitic resistors may not affect the resistor matching condition since both resistors in our circuits are in series to the X-terminals.

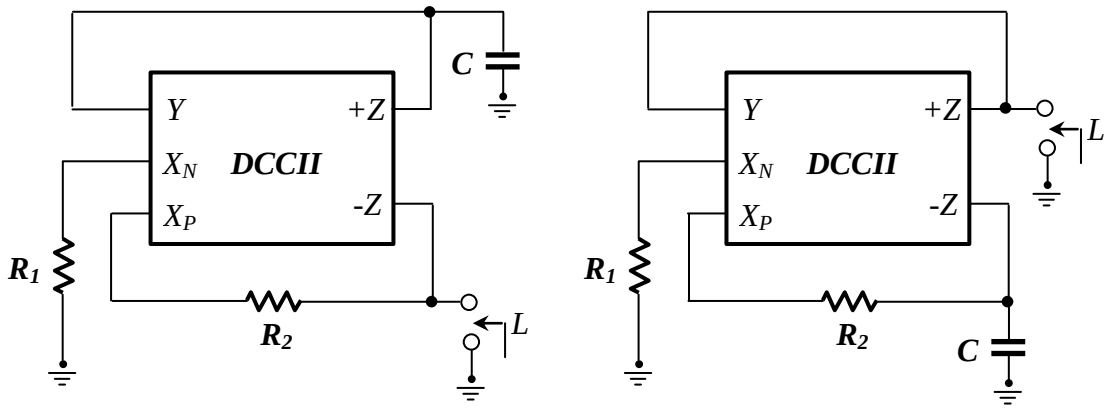


Fig. 3.8. The proposed grounded inductance simulator circuits.

The admittance transfer functions of proposed circuits in Figure 3.8(a) and (b) are given, respectively, for the ideal case ($\beta_1=\beta_2=1$ and $\alpha_N=\alpha_P=1$) as follows

$$Y_a = \frac{1}{R_2 - R_1 + sCR_1R_2} \tag{9}$$

$$Y_b = \frac{1}{sCR_1R_2} + \frac{R_2 - R_1}{R_1R_2} \tag{10}$$

Equations (9) and (10) illustrate that Figure 3.8(a) simulates serial combination of L and R with $R_S=R_2-R_1$ and $L_{eq}=sCR_1R_2$ and Figure 3.8(b) simulates L and R in parallel with $R_p=R_2*R_1/(R_2-R_1)$ and $L_{eq}=sCR_1R_2$. However, pure inductance circuits can be obtained using resistor matching conditions, since it is possible to match resistors with much better precision than 0.1% even in the IC technologies of two decades ago (Gray and Meyer, 1993). For resistor matching condition of $R_1=R_2=R$, we obtain

$$Y = \frac{1}{sL_{eq}} = \frac{1}{sCR^2} \tag{11}$$

In this study a novel inductance simulator circuit is presented. The circuit employs minimum number of elements such, e.g. single differential current conveyor (DCCII), one capacitor and two resistors. The proposed circuit can easily be made electronically tunable by means of one of the resistors is replaced by a MOSFET based tunable resistor (Z. Wang, 1990).

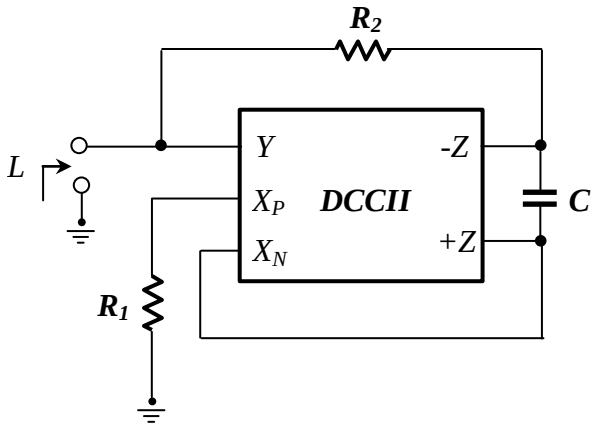


Fig. 3.9. The proposed inductance simulators realized using single DCCII.

The proposed circuit for realizing grounded inductor simulators is shown in Figure 3.9. A routine analysis of the input transfer function is given for the ideal case ($\beta_1=\beta_2=1$ and $\alpha_N=\alpha_P=1$) as follows:

$$Y = \frac{1}{sL_{eq}} = \frac{1}{sCR_1R_2} \tag{12}$$

In this study, the usefulness of the DCCII is shown on six novel lossless grounded inductance simulator circuits. Proposed circuits simultaneously employ minimum number of elements, i.e. single DCCII, one capacitor, and two resistors. No passive element matching restriction is needed and all solutions are electronically tunable in case that one of resistors is replaced by MOSFET based voltage-controlled resistor.

The proposed circuits realizing grounded inductor simulators employing single DCCII, single capacitor, and two resistors are shown in Figures. 3.10 (a)-(f).

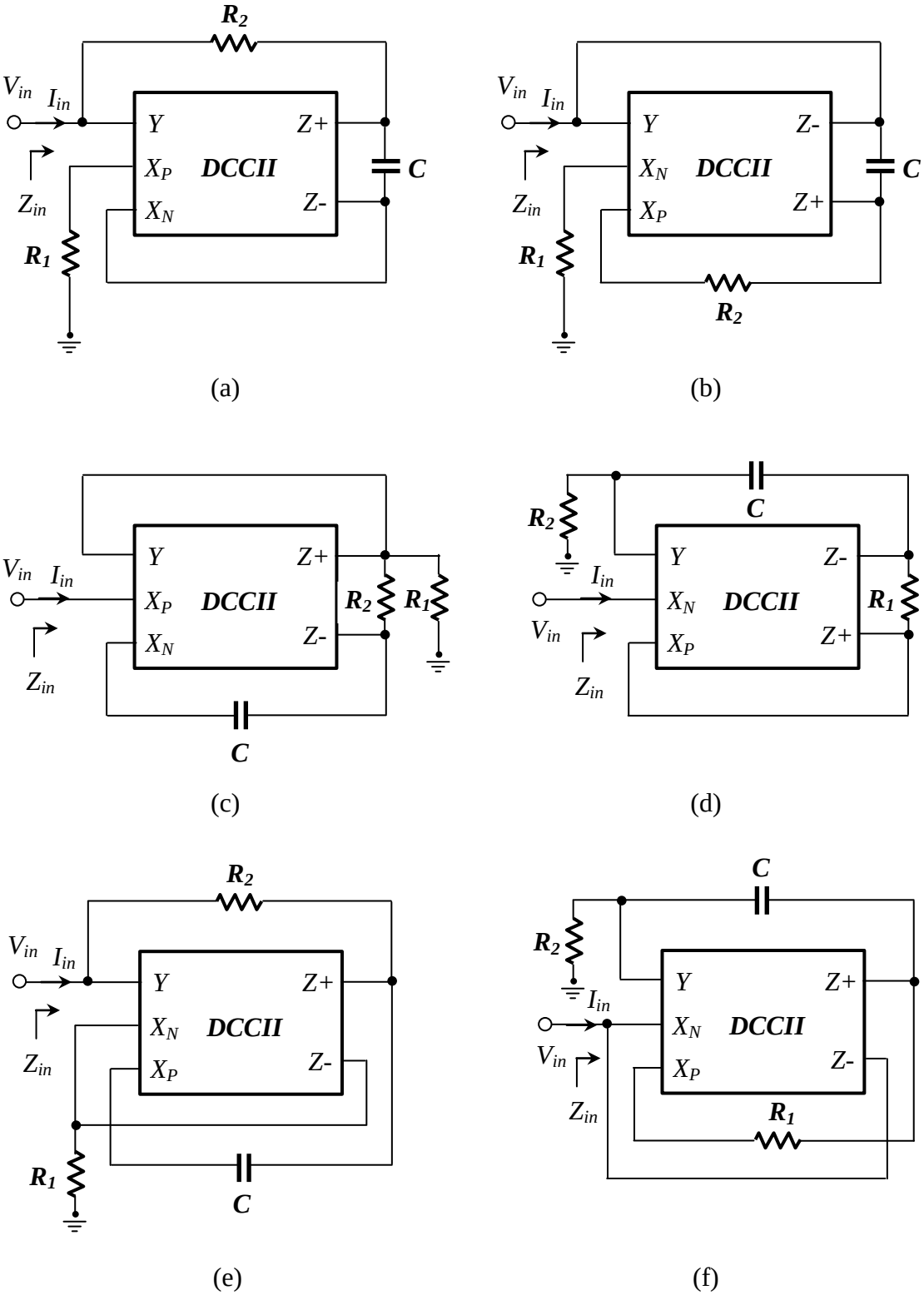


Fig. 3.10. Proposed lossless grounded inductance simulators using single DCCII.

Considering ideal DCCII ($\beta_N=\beta_P=1$ and $\alpha_N=\alpha_P=1$), routine circuit analyses yield the following input impedance for all six variants:

$$Z_{in} = \frac{V_{in}}{I_{in}} = sL_{Eq} = \frac{1}{sCR_1R_2} \tag{13}$$

Passive sensitivities of the proposed circuits are $\left|S^{L_{Eq}}_{R_1,R_2,C}\right| = 1$

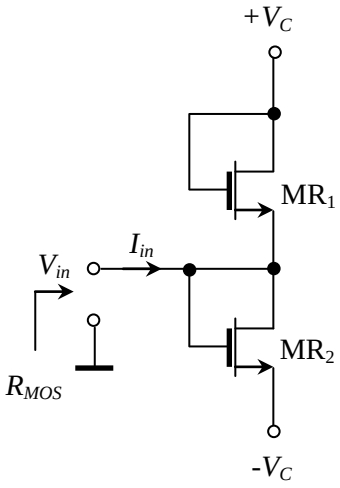


Fig. 3.11. Grounded resistor using two MOSFETs and two symmetrical power supplies.

3.8. DCCII Based Four Quadrant Multiplier

Multipliers are important circuits for implementing various non-linear functions in analog signal processing. A wide range of analog signal processing applications use analog multipliers and dividers such as adaptive filtering, modulation detection, frequency translation and automatic gain controlling and neural networks (K. Bult et al, 1986, Y.K. Seng et al, 1998). Some multipliers use the quadratic relation between drain current and gate-source voltage of the MOS transistors in the saturation region and others use the MOS transistors in the ohmic region (Y.K. Seng et al, 1998).

A new wideband BiCMOS differential current conveyor is presented by Hesham F. Hamed et al, 2001. The proposed differential current conveyor has the advantage of a wide bandwidth (about 1GHz). It can be directly used with MOS transistors operating in the ohmic region to implement the required analogue functions. As an application of the proposed (DCCII) a four quadrant current multiplier is presented using differential current conveyor.

Some multipliers use the quadratic relation between drain current and gate source voltage of the MOS transistors in the saturation region and others use the MOS transistors in the ohmic region. The proposed differential current conveyor can be used to realize multiplier/transconductance cells. A four quadrant multiplier is shown in Figure 3.12 and consists of a differential current conveyor and two MOS transistors operating in the ohmic region.

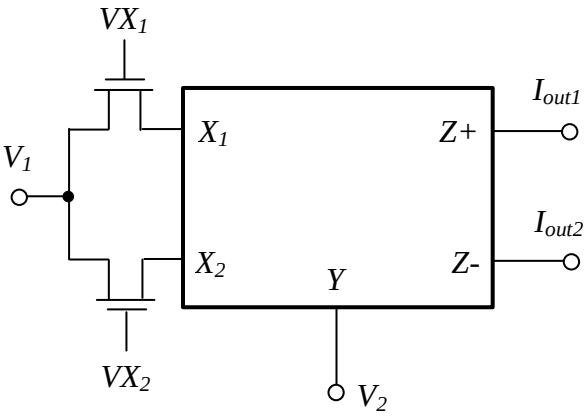


Fig. 3.12. The anlog multiplier using DCCII.

The transconductance multiplying action is achieved by transistors M_1, M_2, which are operating in the ohmic region. The current in the ohmic region that flows through each transistor (M_l, M_2) is given by (H.O Elwan, 1996):

$$I = K(V_G - V_T)(V_D - V_S) + a1(V_D^2 - V_S^2) + a2(V_D^3 - V_S^3) + ... \quad (14)$$

From the characteristics of the differential current conveyor, $V_{x1}=V_{x2}=V_y$ and $I_z=I_{x1}-I_{x2}$. Transistors M_1, M_2 have equal drain and equal source voltages by the action of the DCCII. The output currents I_{out1} and I_{out2} under the condition that M_1 and M_2 are matched are given by:

$$\begin{aligned} I_{out1} &= I_{x1} - I_{x2} \\ &= K(V_{G1} - V_{G2})(V_1 - V_2) \end{aligned} \quad (15)$$

$$\begin{aligned} I_{out2} &= I_{x2} - I_{x1} \\ &= K(V_{G1} - V_{G2})(V_2 - V_1) \end{aligned} \quad (16)$$

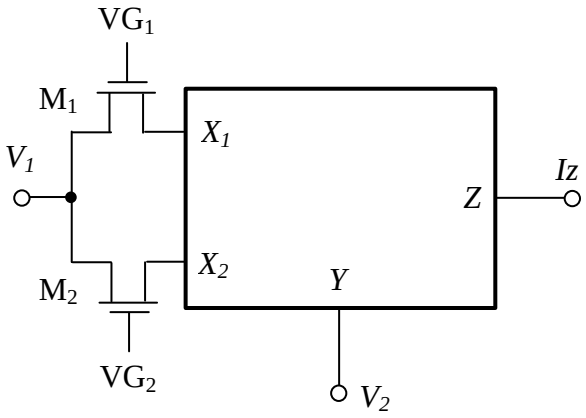


Fig. 3.13. A Four quadrant multiplier using DCCII.

The presented DCCII can be used to realize multiplier/transconductance cells as shown in Figure 3.13. The transconductance multiplying action is achieved by the transistors M_1 and M_2 which are operating in the ohmic region (H.O. Elwan et al, 1996, M. Ismail et al, 1994). The configuration shown cancels both the even and the odd nonlinearities as discussed next.

The current in the ohmic region is given by:

$$I = K(V_G - V_T)(V_D - V_S) + a_1(V_D^2 - V_S^2) + a_2(V_D^3 - V_S^3) + ... \quad (17)$$

Since transistors M1 and M2 have equal drain and equal source voltages by the action of the DCCII therefore the output current $I_Z = I_{X1}$-I_{X2} is given by:

$$I_Z = K(V_{G1} - V_{G2})(V_1 - V_2) \quad (18)$$

Thus the cells can be used as a four quadrant multiplier/transconductance.

3.9. DCCII Based FDNR Circuit Application

A new CMOS high performance dual-X second-generation current conveyor (DXCCII) is presented. The proposed DXCCII provides good linearity, high output impedance at Z terminals, and excellent output–input current gain accuracy. Besides the proposed DXCCII circuit operating at a supply voltage of ±1.5 V. Moreover, a tunable novel lossless frequency-dependent negative resistance (FDNR) circuit employing only a single active element and three passive components is firstly proposed in this study.

The FNDRs are useful elements for the synthesis and design of active filters. The second generation current-conveyors are very attractive for the realization of

FDNRs (Senani R et al, 1984, Nandi S et al, 1984, Abuelma'atti MT et al, 1999, Higashimura M et al, 1987, Higashimura M et al, 1986, Nandi S et al, 1983, Yuce E et al, 2006, Yuce E et al, 2006, Minaei S et al, 2006) as a result of their wider signal bandwidths, greater linearity and larger dynamic range of operation. In this study, to demonstrate circuit synthesis capability of the DXCCII, a tunable lossless FDNR circuit is proposed employing minimum number of active and passive element components. Unlike from other minimal realization (Minaei S et al, 2005), the proposed circuit provides electronic tunability using a triode MOSFET transistor.

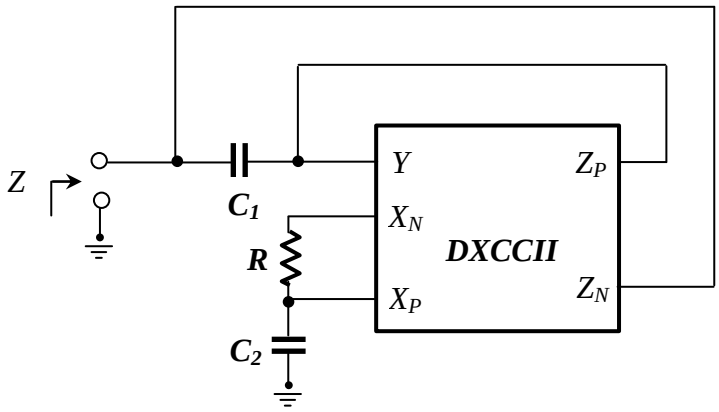
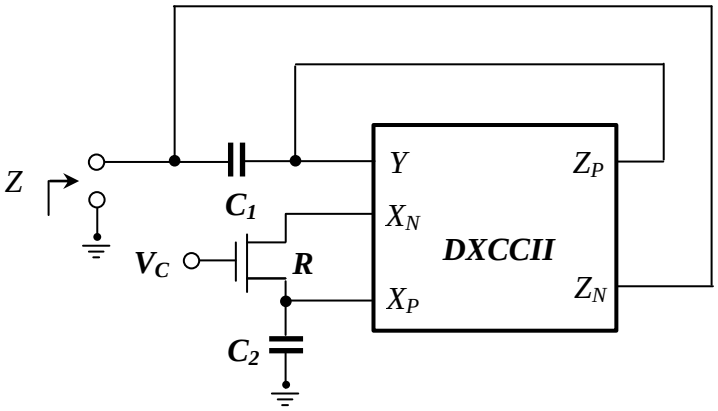


Fig. 3.14. Proposed FDNR realization using a single DXCCII.



The tunable version of the presented FDNR using MOSFET-C technique is shown in Figure 3.15.

The impedance transfer function is given for the ideal case ($\beta 1 = \beta 2 = 1$ and $\alpha_n = \alpha_p = 1$) for C_1=C_2=C as follows:

$$[Z] = \frac{1}{S^2 D_{eq}} = \frac{2}{s^2 C^2 R} \tag{19}$$

3.10. DCCII Based Frequency Compensation methods

A new frequency compensation scheme using a second generation differential current conveyor (DCCII) for three-stage amplifiers is proposed. By adding a DCCII as a feedback path from output of the second and the third stage to the output of the first stage, feed-forward path and the right-half plane zero will be removed subsequently which improves phase margin and the gain-bandwidth product.

To this end, compensation of three-stage amplifiers, Where the amplifier is made up of three gain stages and the second is the only inverting one, the most appropriate solution is the reversed nested Miller compensation (RNMC) (G. Palumbo et al, 2002, R.G.H Eschauzier et al, 1995). RNMC amplifier usually has a better bandwidth than an amplifier with the traditional nested Miller compensation, because the inner compensation capacitor does not load the output node (R.G.H Eschauzier et al, 1995). Nevertheless, conventional RNMC amplifiers are not suitable for low power applications because of their undesired higher order right-half plane (RHP) zero which cause extra power consumption or stability problems. So many RNMC techniques have been reported to cancel the RHP zero (A.D Grasso et al, 2010, K.P Ho et al, 2003, F. Zu et al, 2005, A.D Grasso et al, 2007, A.D Grasso et al, 2004). The presented compensation technique which uses a DCCII block to remove the feed-forward path and the RHP zero thereupon.

In the most of compensation techniques such as NMC and RNMC, compensation network is a feedback and feed-forward path simultaneously. The feed-forward path provides RHP zero, which degenerate frequency response and phase margin mutually. Removing the feed-forward path without attenuation of the feedback can be a solution to obtain suitable frequency response. Voltage and current buffer without influencing feedback path block the feed-forward path and remove undesirable RHP zero completely. However, it is more suitable to use one stage block in the path of Miller capacitors to attain both amplifying feedback and attenuating feed forward path, but the main problem is that the increase in power consumption for adding two blocks is not reasonable. To this end, instead of using two amplifiers or buffers, we can use one DCCII stage in order to buffer two feedback paths and remove

feed-forward. Also it is characterized by transfer function that double pole-zero cancellation occurs that increases the phase margin and gain-bandwidth product.

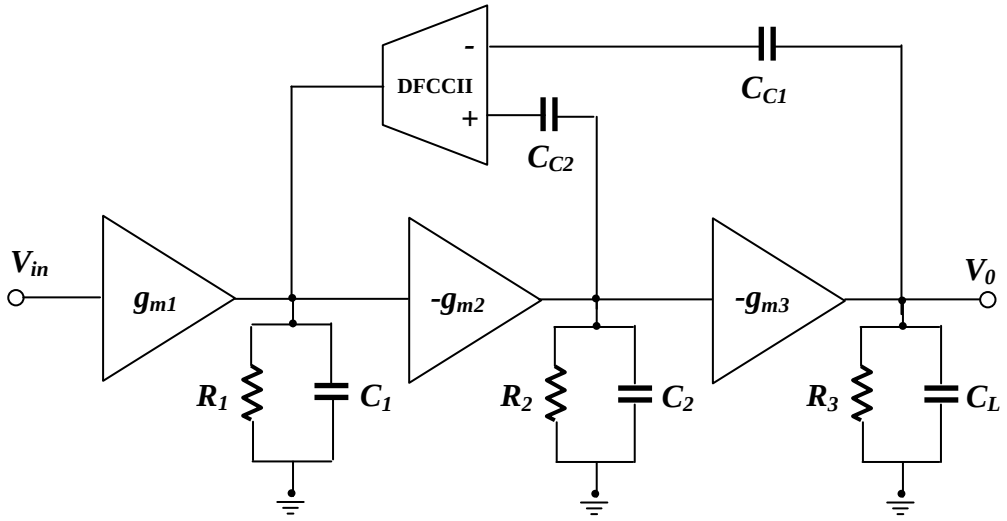


Fig. 3.16. Proposed Compensation Topology.

Figure 3.16 shows linear model of proposed technique. By applying node rule on this model can obtain transfer function of amplifier. In order to reasonably simplify transfer function, the following conditions are assumed:

$$g_{mi}r_i >> 1, \qquad C_L >> C_{C1}, C_{C2} >> C_1, C_2, C_3 \tag{20}$$

By above assumption, the first state open loop transfer function-without series resistors of the proposed amplifier is:

$$H_{OL} = \frac{A_{dc}}{a_2 s^2 + a_1 s + 1} \tag{21}$$

$$A_{dc} = g_{m1}r_1 g_{m2}r_2 g_{m3}r_3$$

$$a_1 = C_{c2} g_{m2} g_{m3} r_1 r_2 r_3$$

$$a_2 = C_L C_{c1} g_{m2} r_1 r_2 r_3$$

According to denominator of open loop transfer function, amplifier has a dominant pole and a non-dominant pole as $P_1$and P_2.

$$P_1 = \frac{1}{C_{C1} g_{m2} g_{m3} r_1 r_2 r_3} \tag{22}$$

$$P_2 = \frac{C_{C1} g_{m3}}{C_{C2} C_L} \tag{23}$$

And the gain bandwidth product is defined as follows:

$$GBW = A_{dc} \cdot P_1 = \frac{g_{m1}}{C_{c1}} \tag{24}$$

3.11. Summary

The introduction of various applications using DCCII as the main active element is given in this chapter. The development of many core applications of the electronic industry are given by using the DCCII viz. all pass filters, band pass filters, multiple output filter, current comparator, inductance simulator, four quadrant multiplier, frequency dependent negative resistance circuits, frequency compensation methods.

CHAPTER IV

DCCII BASED WAVEFORM GENERATORS AND ALL-PASS FILTERS

4.1. Introduction

The DCCII representation of inputs and outputs with corresponding current direction is shown in Figure 4.1. DCCII is a four terminal device among *Y*, X_P and X_N drives, input and the remaining *Z* terminal serve as output. The fundamental property of DCCII is current differencing, which is reflected across *Z* for the input current flowing across X_P and X_N. Furthermore, it offers a high input impedance feature which plays a vital role in the voltage cascading applications, is driven by terminal *Y* across the input. The potential applied across *Y* terminal is being copied to the other input terminals of X_P and X_N.

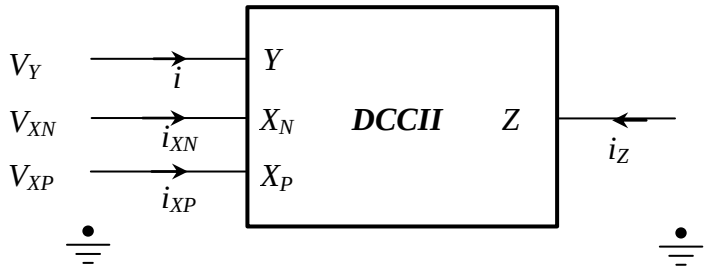


Fig. 4.1. Emblematic depiction of the DCCII input and output terminal currents and voltages.

The hybrid matrix of input and out terminal relation to ideal parameter consideration is presented in (1).

$$\begin{bmatrix} V_{XN} \\ V_{XP} \\ i_Z \\ i_Y \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & 1 \\ 1 & -1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{XP} \\ i_{XN} \\ V_Y \end{bmatrix} \tag{1}$$

From Equation (1), it has been observed that the output current i_Z, is reflected as the difference of input currents X_N and X_P, respectively. Along with the same input potential at the *Y* is driving across the remaining two inputs of X_P and X_N without passing any current through it.

CMOS realization of DCCII as shown in Figure 4.2. The schematic of the DCCII is implemented from Current-controlled (inverting) current differencing buffered amplifier (C-CDBA/C-(I)CDBA) and second-generation current controlled current conveyor (CCCII) structures. It has three sub sections. Firstly, biasing section, done by the transistors M_5-M_{10} and M_{12}. Secondly, translinear loop, in which Y terminal potential is transferred to the other input terminals of X_P and X_N fulfilled by M_1-M_4, M_{18} and M_{19} transistors. Terminal Y has high input impedance which elevates DCCII for applications as amplifier. Finally, major operation of current differencing is attained with the help of remaining transistors of M_{11}, M_{13}-M_{19}, M_{20} and M_{12}.

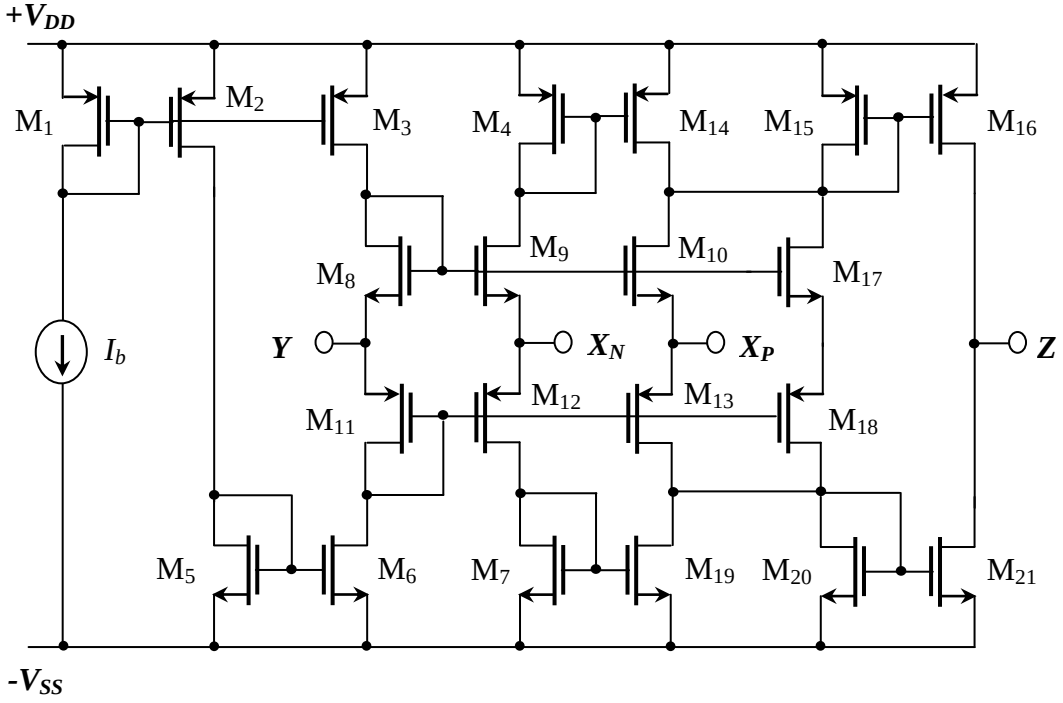


Fig. 4.2. The second generation differential current conveyor circuit diagram. The behavioral model of the DCCII active element is given in Figure 4.3.

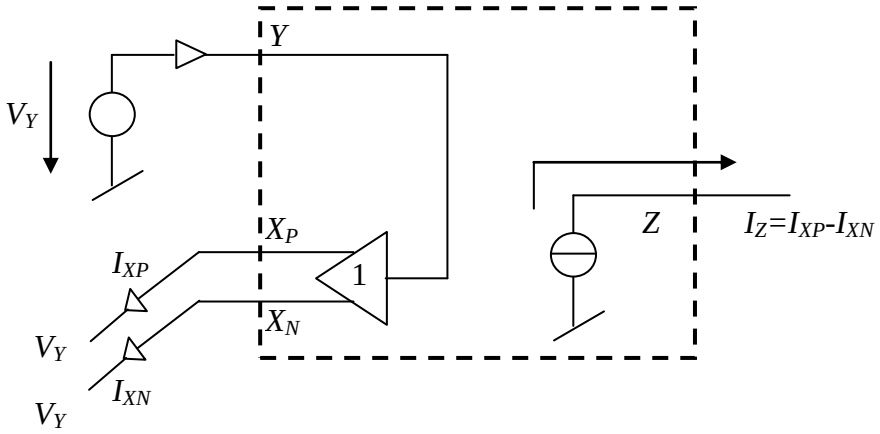


Fig. 4.3. Behavioral model of the DCCII.

4.2. Square Waveform Generators Using Single DCCII

4.2.1. Proposed Square Waveform Generator 1

The proposed square wave generator with single DCCII, two resistors and a grounded capacitor is shown in Figure 4.4.

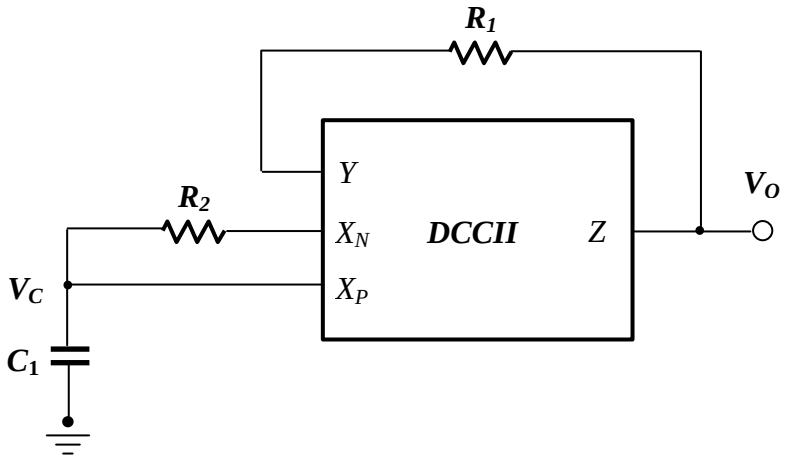


Fig. 4.4. Circuit diagram of proposed square wave generator 1.

The expression for the time period (T) can be derived from the terminal relations of DCCII given in Equation 1 and by applying basic network analysis to the proposed circuit is shown in Figure 4.4.

$$\frac{V_0 - V_Y}{R_1} = I_0 \tag{2}$$

Where 'I_o' is output current. From node V_C,

$$I_{XN} = \frac{V_C - V_{XN}}{R_2} \tag{3}$$

From hybrid matrix (1), can rewrite the above equation as

$$I_{XN} = \frac{V_C - V_Y}{R_2} \tag{4}$$

By applying KCL at node Vc

$$\frac{V_0 - V_{XN}}{R_2} = I_0 \tag{5}$$

$$I_{XN} = \frac{V_C}{R_2} \tag{6}$$

$$I_{XP} = V_{XP} SC \tag{7}$$

Again from Equation (1), can write

$$I_0 = I_{XP} - I_{XN} \tag{8}$$

$$\frac{V_0 - V_C}{R_1} = V_{XP} SC - \frac{V_c}{R_2} \tag{9}$$

From Equation (9)

$$V_0 = V_C R_1 \left(SC - \frac{R_1 + R_2}{R_1 R_2} \right) \tag{10}$$

From, the Equation (2) & (5),

$$V_0 = \left(\frac{1}{R_1} + \frac{1}{R_2} \right) V_C \tag{11}$$

From equating Equation (10) & (11), can obtain S as

$$V_C R_1 \left(SC - \frac{R_1 + R_2}{R_1 R_2} \right) = \left(\frac{1}{R_1} + \frac{1}{R_2} \right) V_C \tag{12}$$

$$S = \frac{(R_1 + R_2)(1 + R_1)}{C R_1^2 R_2} \tag{13}$$

Where $S = j\omega$, and in which ω is the angular frequency in rad/s, from Equation (13), the frequency of operation, can be notated as follows.

$$f = \frac{(R_1 + R_2)(1 + R_1)}{2\pi C R_1^2 R_2} \tag{14}$$

The time period of the proposed circuit at the output terminal V_0 can be expressed as

$$T = \frac{2\pi C R_1^2 R_2}{(R_1 + R_2)(1 + R_1)} \tag{15}$$

4.2.2. Proposed Square Waveform Generator 2

Taking DCCII as a leading component and superficially joined passive components crafted a couple of novel square wave generator circuits is shown in Figure 4.5.

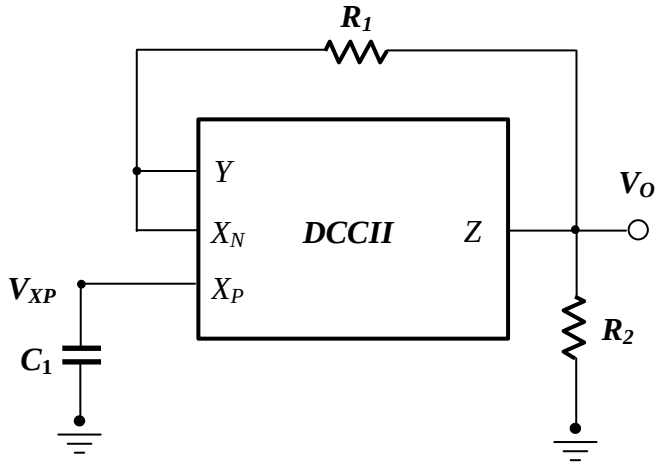


Fig. 4.5. Circuit diagram of proposed square wave generator 2.

Taking DCCII as a leading component and superficially joined passive components crafted a novel square wave generator is shown in Figure 4.5 and offer grounded capacitor.

Let us consider the ideal terminal characteristics of the DCCII documented in Equation (1). Referring to the notations as shown in Figure 4.1 and for ideal DCCII, $i_z=i_{XP}-i_{XN}$ and $V_{XP}=V_{XN}=V_Y$, therefore i_{XP} flows out of the node X_P as shown in Figure 4.5.

From Figure 4.5, $V_o = V_{XP}.\dfrac{R_2}{R_1+R_2}$ and $V_{XP} = \beta V_o$ (16)

The voltage across the capacitor as a function of time is given by

$$V_c(t) = V_f + (V_i - V_f)\exp(-t/R_1C) \tag{17}$$

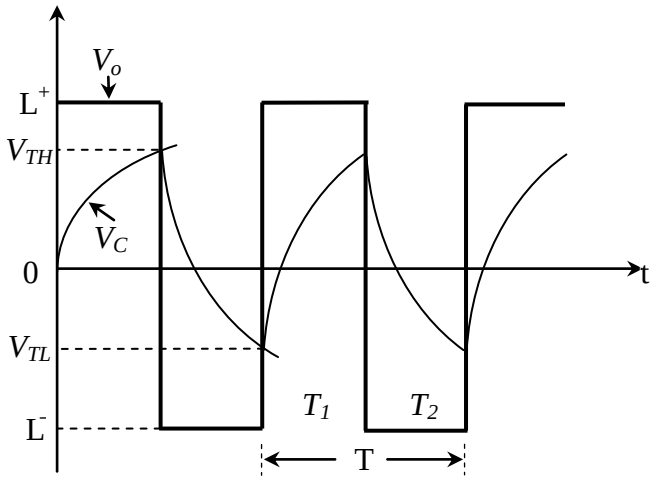


Fig. 4.6. Waveforms of the proposed circuit shown in Figure 4.5.

From Figure 4.6 where V_{XP} is the voltage charging the capacitor linearly to give rise to a triangular waveform. Where final value, $V_f = +V_0$ and initial value $V_i=-\beta V_0=-\beta V_{DD}$.

Therefore, at t=T, $V_C(t)=\beta Vo$

$$\beta V_{DD} = V_{DD} + (-\beta V_{DD} - V_{DD})\exp(-t/R_1C) \tag{18}$$

Solving Equation (18) we can get the expression for the time period of the waveform generator which can be written as

$$T = 2R_1C\ln\left(\frac{1+\beta}{1-\beta}\right) \tag{19}$$

4.2.3. Proposed Square Waveform Generator 3

Considering DCCII as a principle device and with externally attached passive components of two resistors and a capacitor, one new square waveform generator is proposed, is shown in Figure 4.7.

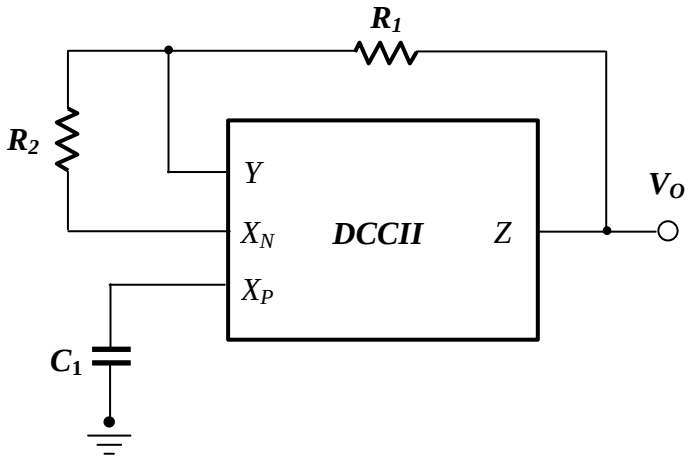


Fig. 4.7. Circuit diagram of proposed square wave generator 3.

From the equalities of DCCII shown in Equation (1) and by applying basic network analysis, the mathematical relation of the Figure 4.8 with respect to the superficially joined capacitors and resistors is written as follows.

$$sCR_1R_2 - (R_2 - 1) = 0 \tag{22}$$

with $s = j\omega$, where ω is the angular frequency in rad/s, the oscillation frequency (*f*) can be expressed from (2). The Equation (22) is derived with the actual current directions taken from Figure 4.7 and from the device properties shown in Equation (1). From Equation (22), the time period of the proposed square waveform generator is derived in Equation (23).

$$T = \frac{2\pi CR_1R_2}{R_2 - 1} \tag{23}$$

The Frequency of oscillation for the proposed model from the above Equation (23) is given as in Equation (24).

$$f = \frac{R_2 - 1}{2\pi CR_1R_2} \tag{24}$$

4.3. All-pass Filter Circuits

4.3.1. Proposed All-Pass Filter 1

The proposed all-pass filter with single DCCII, two resistors and two capacitors is shown in Figure 4.8. Using basic network analysis of the circuit, the required mathematical formation for its transfer function is derived as follows.

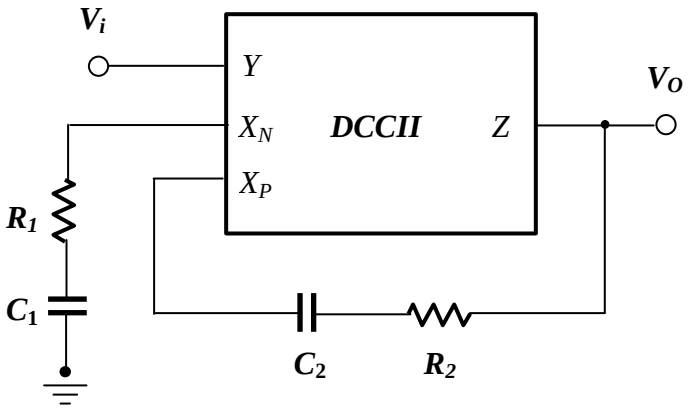


Fig. 4.8. Circuit diagram of proposed All-Pass Filter 1.

The deviation for transfer function for the proposed circuit shown in Figure 4.8, can be expressed as follows:

By considering,

$$Z_1 = \frac{R_1 C_1 S + 1}{C_1 S} \tag{28}$$

And

$$Z_2 = \frac{R_2 C_2 S + 1}{C_2 S} \tag{29}$$

From input node,

$$I_{X_N} = \frac{-C_1 S V_i}{R_1 C_1 S + 1} \tag{30}$$

The current across output node,

$$I_Z = \frac{V_i - V_0}{Z_2} \tag{31}$$

$$I_Z = \frac{(V_i - V_0) C_2 S}{(R_2 C_2 S + 1)} \tag{32}$$

And the output current can be expressed as

$$I_{X_P} = -I_Z \tag{33}$$

And from the hybrid matrix of Equation (33)

$$I_Z = I_{X_P} - I_{X_N} \tag{34}$$

From Equation (33) and (34)

$$2I_Z = -I_{X_N} \tag{35}$$

By substituting Equation (30) in Equation (35), can obtain output current as

$$I_Z = \frac{(C_1 S)V_i}{2(R_1 C_1 S + 1)} \tag{36}$$

By equating Equation (33) and (36)

$$V_i\left[\frac{2C_2(R_1C_1S+1) - C_1(R_2C_2S+1)}{2(R_1C_1S+1)C_2}\right] = V_0 \tag{37}$$

And finally, the transfer function can be obtained as

$$\frac{V_0}{V_i} = \frac{2C_2(R_1C_1S+1) - C_1(R_2C_2S+1)}{2C_2(R_1C_1S+1)} \tag{38}$$

The proposed filter should satisfy the following conditions in order to work as an all-pass filter application.

For R_2=3R, R_1=R and C_1=C_2

$$\frac{V_0}{V_i} = \frac{1}{2}\left(\frac{1 - sRC}{1 + sRC}\right) \tag{39}$$

4.3.2. Proposed All-Pass Filter 2

In similar to the earlier circuit realization another all pass filter circuit is implemented as shown in Figure 4.9. The mathematical model for the proposed circuit's transfer function can be derived as follows.

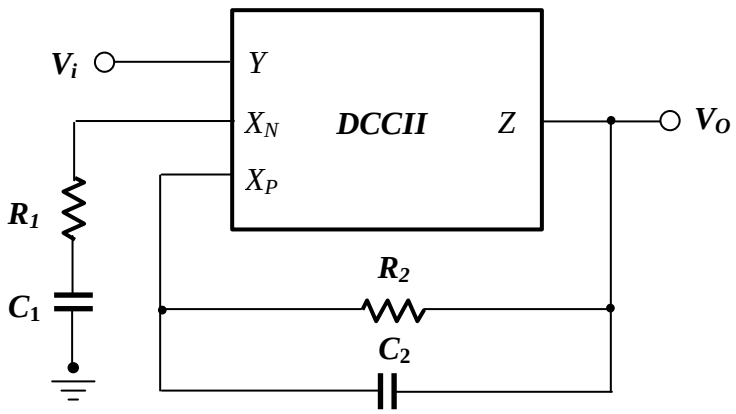


Fig. 4.9. Circuit diagram of proposed All-Pass Filter 2.

The mathematical expression for the voltage transfer function can be written as follows for the circuit shown in Figure 4.9.

By considering,

$$Z_1 = R_1 + \frac{1}{sC_1} = \frac{sRC_1 + 1}{sC_1} \tag{40}$$

And

$$Z_2 = \frac{R_2 \times 1/sC_2}{R_2 + 1/sC_2} = \frac{R_2}{sR_2C_2 + 1} \tag{41}$$

From input node,

$$I_{X_N} = \frac{-Vin}{Z_1} = \frac{-Vin(sC_1)}{(sR_1C_1 + 1)} \tag{42}$$

$$I_{Xp} = \frac{Vout - Vin}{Z_2} = \frac{(Vout - Vin)}{R_2}(sR_2C_2 + 1) \tag{43}$$

$$I_Z = -i_{Xp} = \frac{-(Vout - Vin)}{R_2}(sR_2C_2 + 1) \tag{44}$$

$$\frac{-(Vout - Vin)}{R_2}(sR_2C_2 + 1) = \frac{(Vout - Vin)}{R_2}(sR_2C_2 + 1) + \frac{Vin(sC_1)}{sR_1C_1 + 1} \tag{45}$$

$$\frac{-2(Vout - Vin)(sR_2C_2 + 1)}{R_2} - \frac{Vin(sC_1)}{sR_1C_1 + 1} = \frac{2Vout(sR_2C_2 + 1)}{R_2} \tag{46}$$

$$Vin\left[\frac{2(sR_2C_2 + 1)}{R_2} - \frac{(sC_1)}{sR_1C_1 + 1}\right] = \frac{2Vout(sR_2C_2 + 1)}{R_2} \tag{47}$$

$$\frac{2(1 + sR_2C_2)(sR_1C_1 + 1) - sR_2C_1}{R_2(sR_1C_1 + 1)} = \frac{2Vout(sR_2C_2 + 1)}{R_2} \tag{48}$$

And finally, the transfer function can be obtained as

$$\frac{V_0}{V_i} = \frac{2(1 + sR_2C_2)(1 + sR_1C_1) - sR_2C_1}{2(sR_1C_1 + 1)(sR_2C_2 + 1)} \tag{49}$$

The proposed filter should satisfy the following conditions in order to work as an all-pass filter application.

For R_2=R, R_1=R/8, C_1=C and C_2=C/8

$$\frac{V_0}{V_i} = \left(\frac{s^2R^2C^2 - 16sRC + 64}{s^2R^2C^2 + 16sRC + 64}\right) \tag{50}$$

4.3.3. Proposed All-Pass Filter 3

The third realization of the all pass filter circuit using single DCCII, two resistors and two capacitors is given in the Figure 4.10. In the similar pattern to that of previous derivations, the mathematical description for the introduced model is given in the following equations.

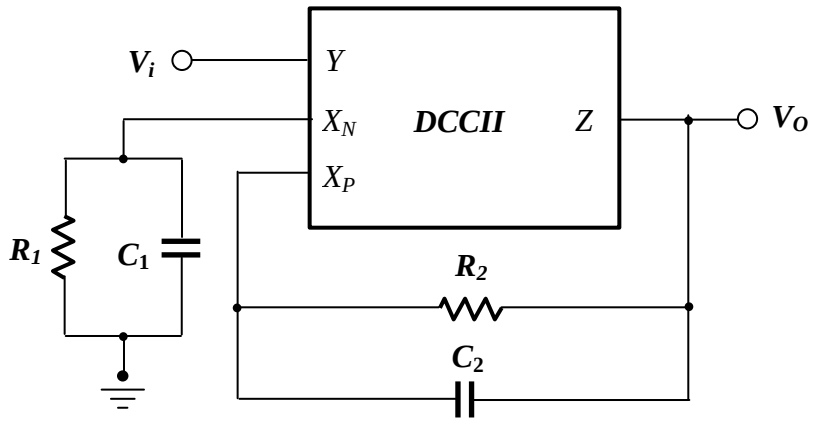


Fig. 4.10. Circuit diagram of proposed All-Pass Filter 3.

From the circuit shown in Figure 4.10, the expression for the voltage transfer function can be derived as follows:

By considering,

$$Z_1 = \frac{R_1 \times 1/sC_1}{R_1 + 1/sC_1} = \frac{R_1}{sR_1C_1 + 1} \tag{51}$$

$$Z_1 = \frac{R_2 \times 1/sC_2}{R_2 + 1/sC_2} = \frac{R_2}{sR_2C_2 + 1} \tag{52}$$

$$\frac{Vo}{Vin} = \left(\frac{2Z_1 - Z_2}{2Z_1}\right) = \frac{2\left(\frac{R_1}{sR_1C_1 + 1}\right) - \frac{R_2}{sR_2C_2 + 1}}{2\left(\frac{R_1}{sR_1C_1 + 1}\right)} \tag{53}$$

$$\frac{Vo}{Vin} = \frac{2R_1(sR_2C_2 + 1) - R_2(sR_1C_1 + 1)}{2R_1(sR_2C_2 + 1)} \tag{54}$$

And finally, the transfer function can be obtained as

$$\frac{V_0}{V_i} = \frac{sR_1R_2(2C_2 - C_1) + (2R_1 - R_2)}{2R_1(sR_2C_2 + 1)} \tag{55}$$

The proposed filter should satisfy the following conditions in order to work as an all-pass filter application.

For R_2=3R, R_1=R and C_1=C, C_2=C/3

$$\frac{V_0}{V_i} = \frac{1}{2}\left(\frac{1-sRC}{1+sRC}\right) \tag{56}$$

4.4. Summary

The analytical model of the proposed device and the corresponding applications are presented in this chapter. By considering the behavioural property of the device and the influence of the transistors behaviour in the saturation region with the help of basic network laws the required mathematical expressions for the elevated applications are derived and are given in this chapter.

CHAPTER V

DCCII BASED WAVEFORM GENERATORS AND ALL-PASS FILTERS: SIMULATION RESULTS

5.1. Introduction

In this chapter, the simulation results for the newly proposed circuits in the chapter 4 using single DCCII active elements are given. All the proposed circuits given in chapter 4 are designed using one DCCII along with few passive components. All the proposed circuits are simulated for waveform generation by using the CMOS DCCII shown in Figure 5.1. The CMOS DCCII shown in Figure 5.1 is designed using Cadence 180 nm CMOS model parameters and simulated by using SPECTRE simulation model parameters. For simulation, the supply voltages ± 2.5 V are used for all the proposed circuits.

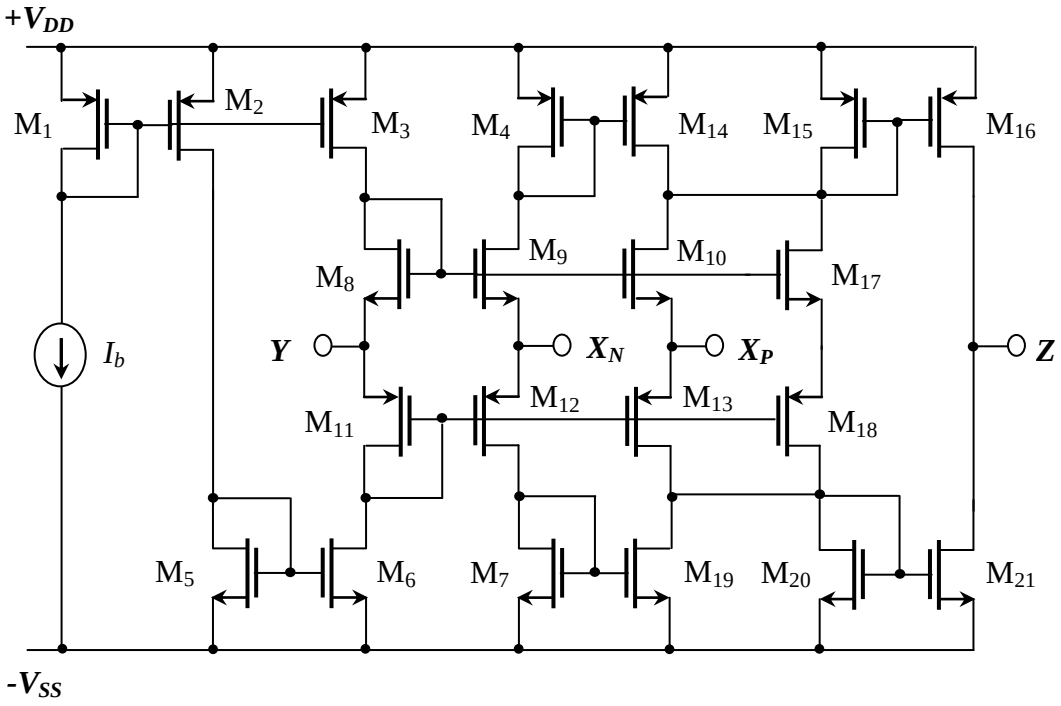


Fig. 5.1. The second generation differential current conveyor circuit diagram.

The transistors widths and lengths used for simulating the CMOS DCCII by Cadence gpdk 180 nm are given in Table 5.1 and the bias current used during the simulation is I_o = 400 µA.

The design parameters of CMOS DCCII as shown in Figure 5.1 are tabulated in Table 1.

Table 5.1 The Transistors Aspect Ratios of the circuit shown in Figure 5.1.

Transistor	***W (µm)***	***L (µm)***
M_3, M_4, M_{19}, M_{20}	50	0.35
M_5-M_7	30	2.0
M_{12}, M_{13}, M_{16}	30	1.0
M_{17}	50	2.0
M_1, M_2, M_{18}, M_{21}	20	0.35
M_8, M_9	10	2.0
M_{10}, M_{11}, M_{14}	10	1.0
M_{15}	20	2.0

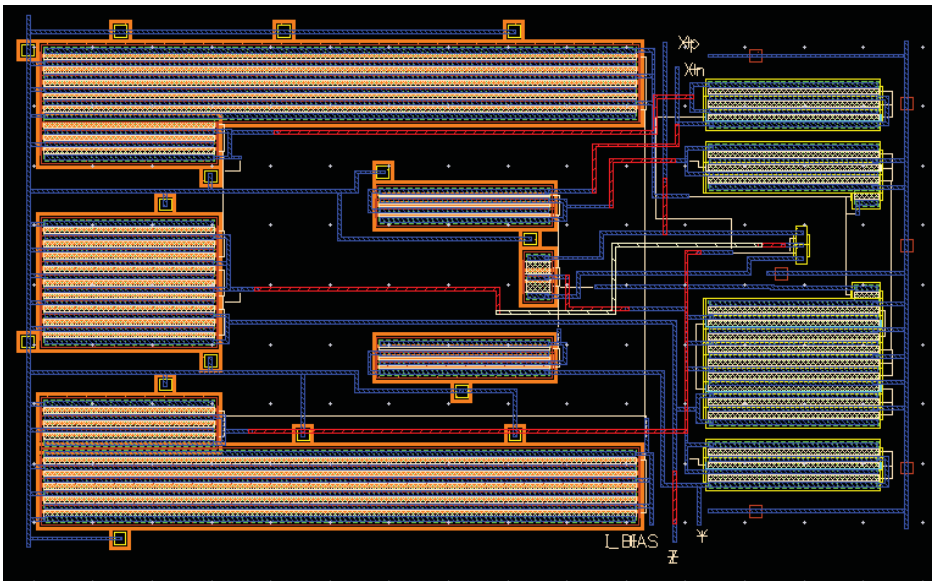


Fig. 5.2. Layout of the DCCII shown in the Figure 5.1.

Figure 5.2 shows the layout of the second generation differential current conveyor of Figure 5.1 with the optimized chip area of 3334.07 µm^2 and has used three metal layers for making interconnections between nets and instances of circuit, it is designed using Cadence Virtuoso with the help of gpdk 180 nm technology. And its GDSII file has successfully generated by using Cadence Assura with zero violations in

Design Rule Check (DRC), matched Layout Vs Schematic (LVS) and RCX parasitic extraction of resistances and capacitances.

5.2. Square Waveform Generators Using Single DCCII

5.2.1. Simulation Results

5.2.1.1. Proposed Square Waveform Generator 1

The testing of the proposed square wave generator is shown in Figure 5.3 has done by using Cadence spectre simulation model parameters.

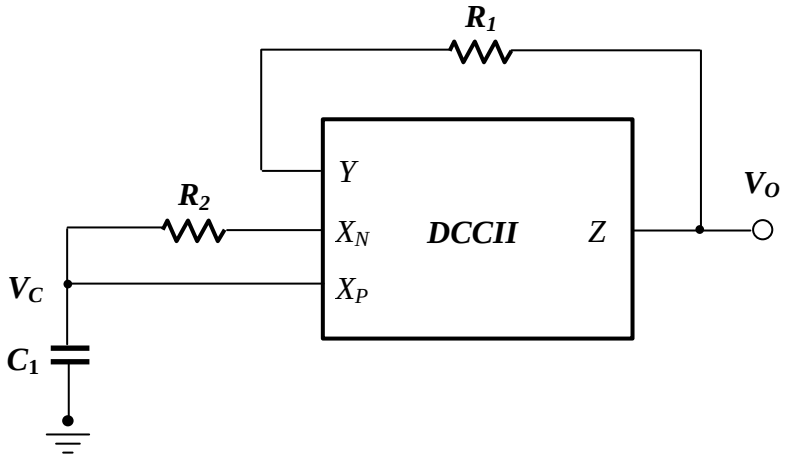


Fig. 5.3. Circuit diagram of proposed square wave generator 1.

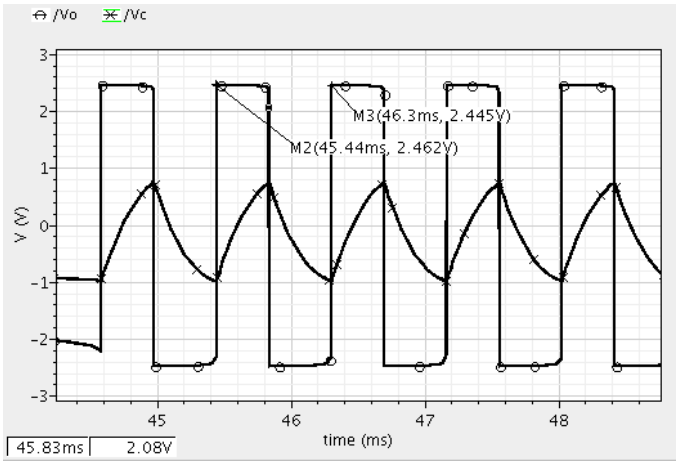


Fig. 5.4. The output waveform across output and capacitor node of the proposed square wave generator 1.

Figure 5.4 depicts the typical output waveforms of the proposed square wave generator with charging-discharging across the capacitor. The taken values of the passive components in faithful output is R_1 = 50 kΩ, R_2 = 3 kΩ, and C = 100 nF. The measured time period of the output waveform is T= 0.86 ms.

The linear variation of the time period against the variation of capacitor by fixing R_1 = 50 kΩ, R_2 = 3 kΩ is shown in Figure 5.5. The variation of capacitor value is from 1nF to 0.4 μF.

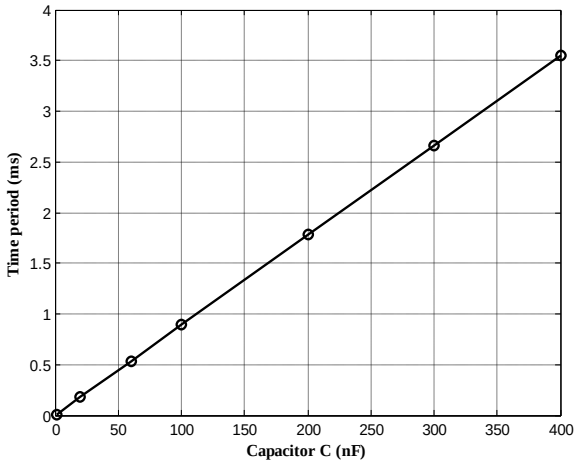


Fig. 5.5. The graph of Time period (T) Vs Capacitor (C) at R_1 = 50 kΩ and R_2= 3 kΩ.

Similarly, by maintaining R_1 = 50K and C = 100 nF the variation of the time period against the value of Resistor R_2 can be plotted is shown in Figure 5.6.

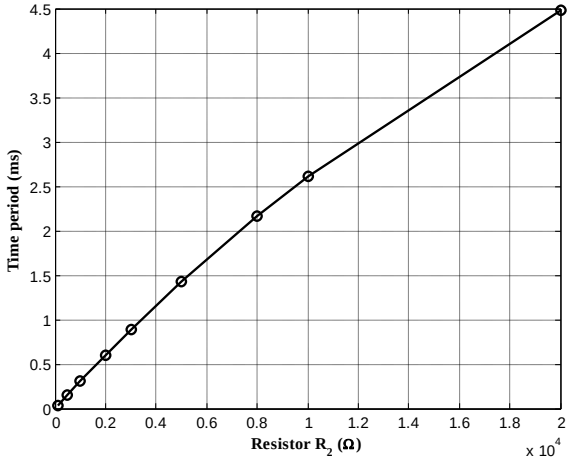


Fig. 5.6. The graph of Time period (T) Vs Resistor R_2 at C = 100 nF and R_1 = 50 kΩ.

The variation of the time period against the value of Resistor R_1 is shown in Figure 5.7. For this task, R_1 varies within the range of a few ohms to few kilo ohms by keeping the other components at C = 100 nF and R_2 = 3 KΩ.

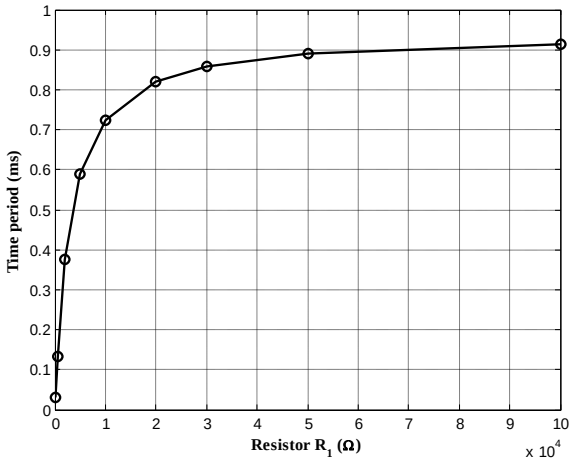


Fig. 5.7. The graph of time period (T) Vs resistor R_1 at C = 100 nF and R_2 = 3 kΩ.

For simulation and tunability, the supply voltage of ±2.5 V has considered with a biasing current of 400 µA.

5.2.1.2. Proposed Square Waveform Generator 2

Using Cadence Virtuoso, Circuit shown in Figure 5.8 is simulated by considering gpdk 180 nm technology spectre files. For these circuits the required supply voltage of ±2.5 V where as 400 µA for bias current are taken.

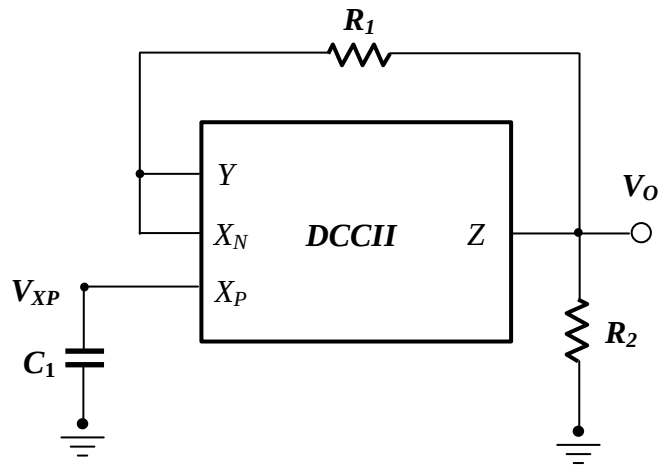
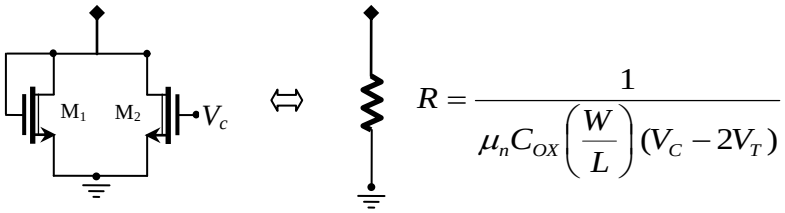


Fig. 5.8. Circuit diagram of proposed square wave generator 2.

A linear resistor can be realized by using a parallel connection of two depletion type NMOS transistors operated in the triode region as illustrated in below Figure 5.9 (A. Gökçen et al, 2010). This method cancels out the non-linearity of the MOSFET significantly.



$$R = \frac{1}{\mu_n C_{OX}\left(\frac{W}{L}\right)(V_C - 2V_T)}$$

Fig. 5.9. Linear resistor realization using two NMOS transistors.

The simulated outputs of Figure 5.8 proposed circuit, is shown in Figure 5.10. The circuit output is generated with the selected values of R_1 = 5 kΩ, R_2 = 15 kΩ and C = 10 nF.

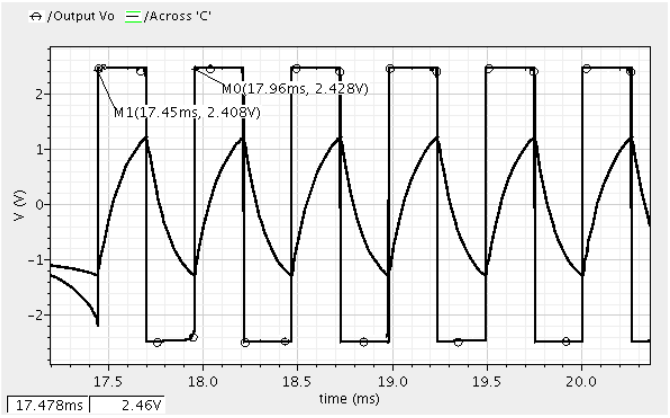


Fig. 5.10. The output waveform across output and capacitor node of the proposed square wave generator 2.

The linearity of the proposed circuit with respect to the capacitor variation is shown in Figure 5.11. The capacitor is varied from 1 nF to 1 µF by maintaining other two external components at R_1 = 5 kΩ, R_2 = 15 kΩ.

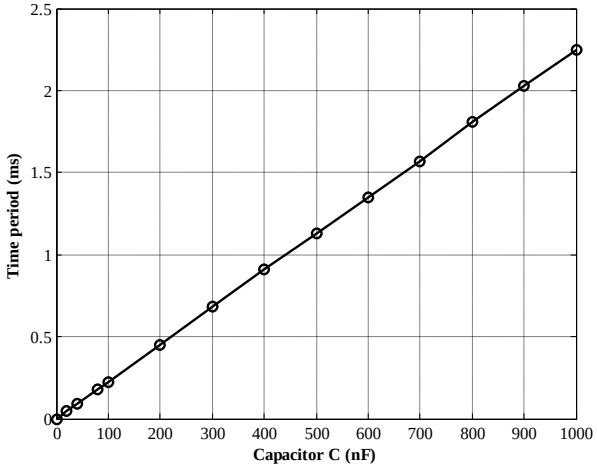


Fig. 5.11. Time period (T) variation with respect to Capacitor C by forcing R_1 = 5 kΩ and R_2 = 15 kΩ.

Similarly, the variation of the time period in contrast to R_2 for the proposed model is plotted in Figure 5.12. In doing so, the circuit is forced to R_1 at 5 kΩ and C at 10 nF.

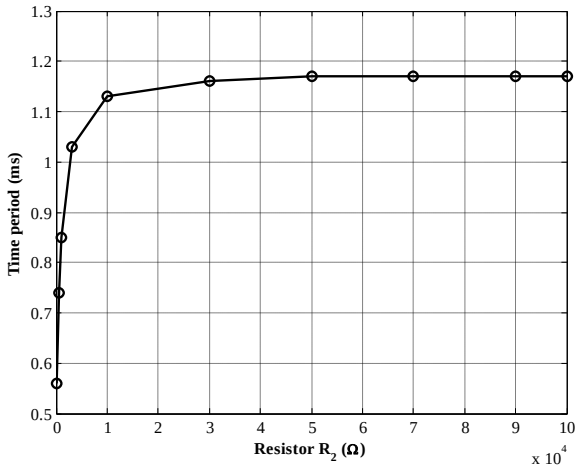


Fig. 5.12. Representation of Time period (T) Vs Resistor R_2 with C = 10 nF and R_1=5kΩ.

In the same way, the response of time period in accordance with R_1 for the invented circuits is presented in Figure 5.13. For achieving this, the circuit values are kept at R_1 = 15 kΩ and C = 100 nF.

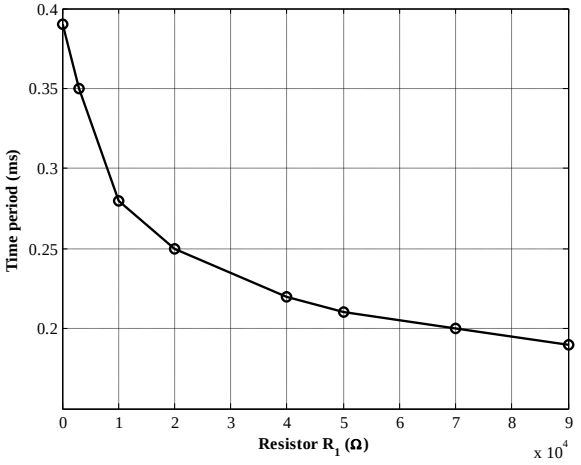


Fig. 5.13. Representation of Time period (T) Vs Resistor R_1 with C = 10 nF and R_2=15 kΩ.

5.2.1.3. Proposed Square Waveform Generator 3

The simulation setup of Figure 5.14 is carried out in Cadence virtuoso using gpdk 180 nm spectre model libraries at ±2.5 V of supply voltage and biasing current of 400 µA are considered.

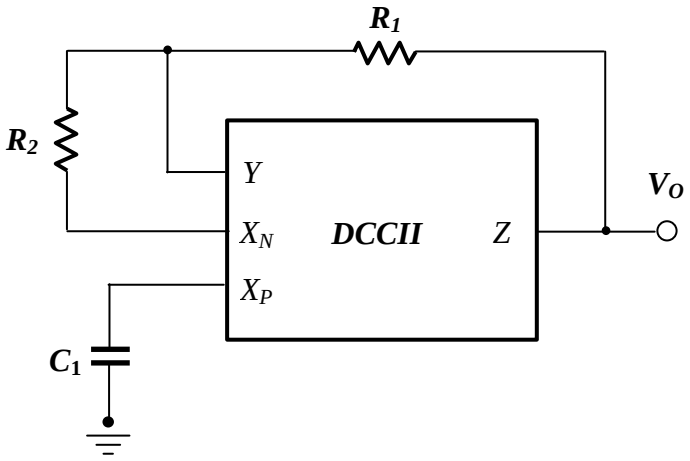


Fig. 5.14. Circuit diagram of proposed square wave generator 3.

The resultant simulation output of spectre simulation is presented in Figure 5.14. Design parameters of the proposed structure in order to satisfy the mathematical model and hardware results are R_1 = 0.5 kΩ, R_2 = 10 kΩ and C = 50 nF respectively.

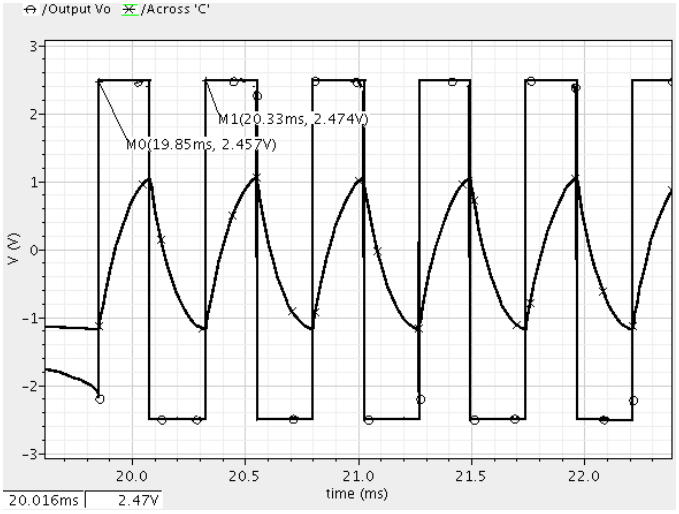


Fig. 5.15. The output waveform across output and capacitor node of the proposed square wave generator 3.

The impact of capacitor sweeping on time period is given in Figure 5.16. From this, the circuit's linearity over the range of capacitance is attained. To acquire this smooth functionality the other parameters of R_1 = 0.5 kΩ and R_2 = 10 kΩ are chosen.

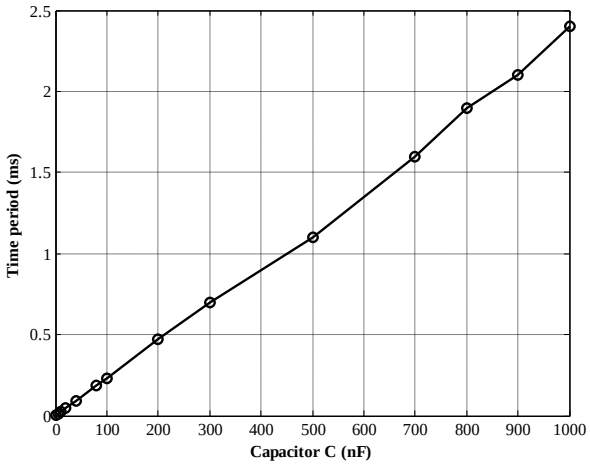


Fig. 5.16. The Linearity curve representing the variation of Time period (T) with respect to Capacitor (C).

The observation of the time period (T) versus resistor R_2 is shown in Figure 5.17 keeping other passive components at R_1 and C at 10 kΩ and 50 nF, respectively.

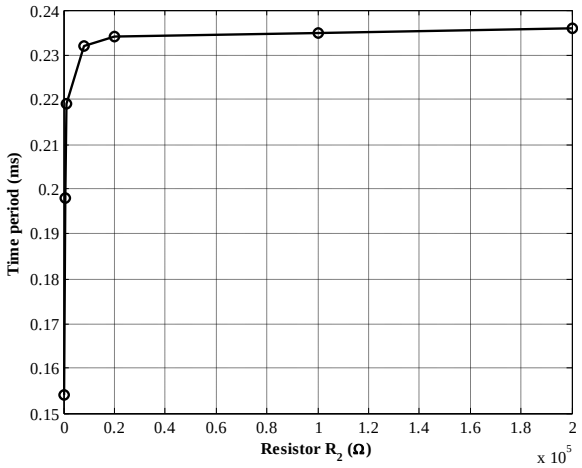


Fig. 5.17. Illustration of Time period (T) with Resistor R_2.

In similar to the previous curves, Figure 5.18 presents the left over the depiction of resistor R_1 to the time period by forcing R_1 = 0.5 kΩ and C = 50 nF.

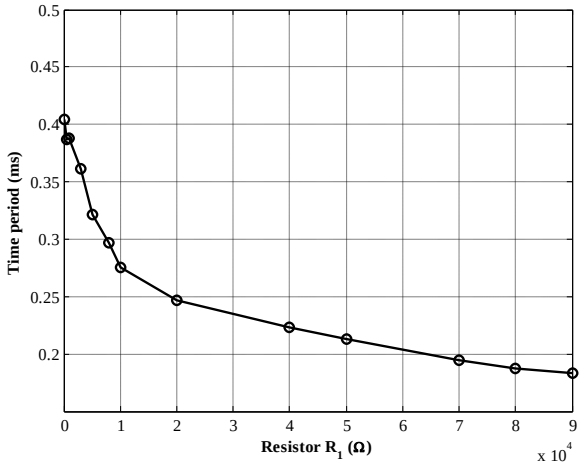


Fig. 5.18. The graph representing Time period (T) Vs Resistor R_1.

5.3. All-pass Filter Circuits

5.3.1. Simulation Results

5.3.1.1. Proposed All-Pass Filter 1

The theoretical model of the proposed circuit is developed in Cadence Virtuoso environment and simulated using spectre model parameters.

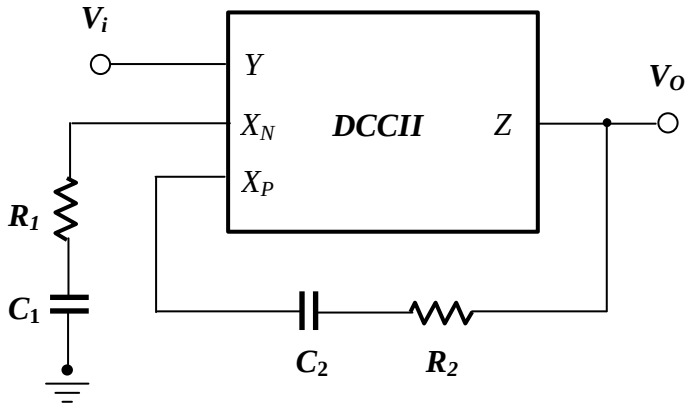


Fig. 5.19. Circuit diagram of proposed All-Pass Filter 1.

The simulated response of the proposed all-pass section across the input and output terminal is shown in Figure 5.20.

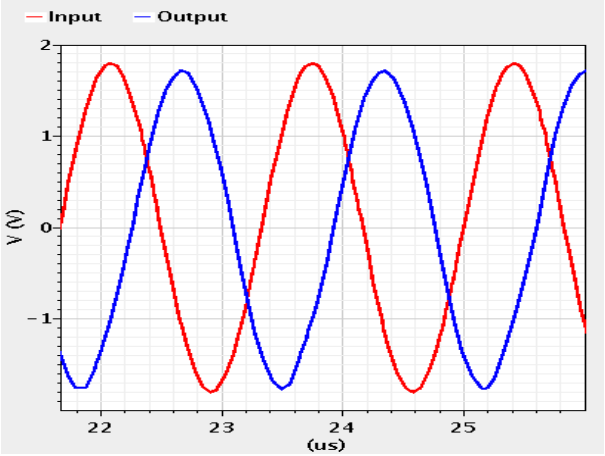


Fig. 5.20. The simulated response of proposed all-pass filter as shown in Figure 5.19.

For the model shown in Figure 5.19, the designing parameters can be disclosed as equal to passive component are R_1 = 12.6 kΩ, R_2 = 1 kΩ, and C_1 = 1 uF and C_2 = 100 pF. The supply voltage and biasing current for the above mentioned circuit as shown in Figure 5.19 are ± 2.5 V and 400 µA respectively.

5.3.1.2. Proposed All-Pass Filter 2

The simulated response of the proposed all-pass section across the input and output terminal is shown in Figure 5.22.

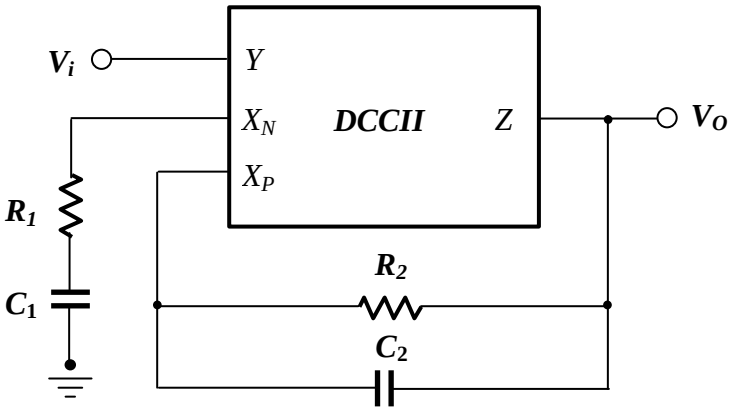


Fig. 5.21. Circuit diagram of proposed All-Pass Filter 2.

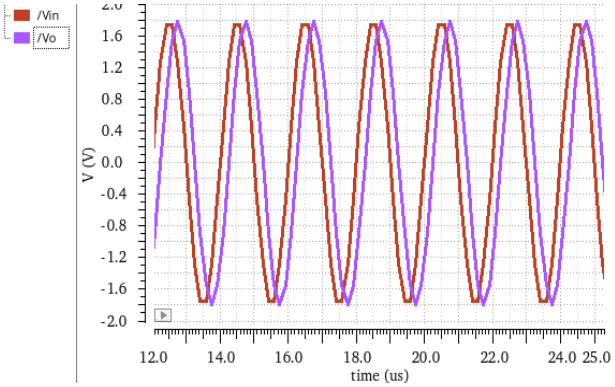


Fig. 5.22. The simulated response of proposed all-pass filter as shown in Figure 5.21.

For the model shown in Figure 5.21, the designing parameters can be disclosed as equal to passive component are R_1 = 24.5 kΩ, R_2 = 5 kΩ, and C_1 = 100 uF and C_2 = 10 pF. The supply voltage and biasing current for the above mentioned circuit as shown in Figure 5.21 are ± 2.5 V and 400 µA respectively.

5.3.1.3. Proposed All-Pass Filter 3

The theoretical model of the proposed circuit is developed in Cadence Virtuoso environment and simulated using spectre model parameters.

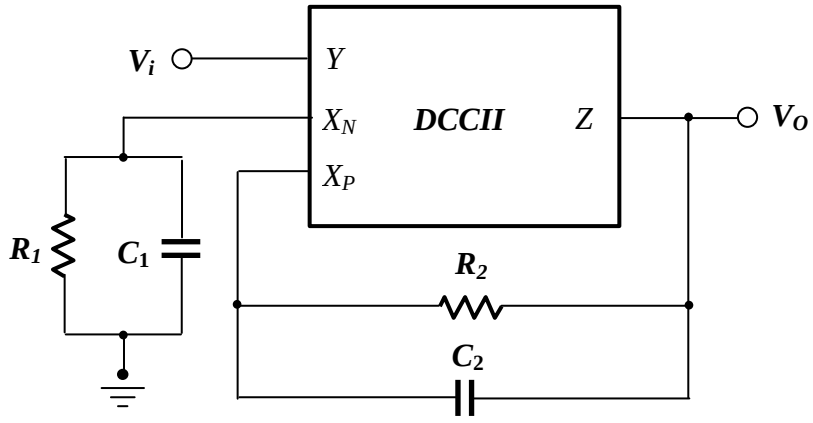


Fig. 5.23. Circuit diagram of proposed All-Pass Filter 3.

The simulated response of the proposed all-pass section across the input and output terminal is shown in Figure 5.24.

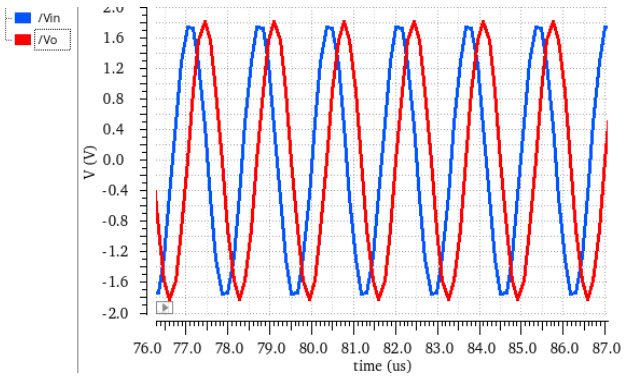


Fig. 5.24. The simulated response of proposed all-pass filter as shown in Figure 5.23.

For the model shown in Figure 5.23, the designing parameters can be disclosed as equal to passive component are R_1 = 38.6 kΩ, R_2 = 1 kΩ, C_1 = 1 uF and C_2 = 100 pF. The supply voltage and biasing currents for the above mentioned circuit as shown in Figure 5.23 are ± 2.5 V and 400 µA respectively.

5.4. Summary

The theoretical development of the proposed circuits mathematical model is constructed using CMOS realization and the same is designed and tested in the cadence virtuoso environment with the usage of gpdk 180 nm technology library files. The proposed circuits shows approximately close values to the analytical model during simulation and the corresponding values and plots are presented in this chapter.

CHAPTER VI

DCCII BASED WAVEFORM GENERATORS AND ALL-PASS FILTERS: EXPERIMENTAL RESULTS

6.1. Introduction

In this chapter, the experimental results for the proposed circuits in chapter 4 are given. All the proposed circuits are tested for waveform generation on a laboratory breadboard by using a prototype DCCII circuit. The prototype DCCII circuit is designed by using two AD844AN ICs (C.L Hou et al, 2005, Y.K. Lo et al, 2007a, Y.K. Lo et al, 2007b, Y.K. Lo et al, 2006). The IC AD844AN is a high speed monolithic current feed-back operational amplifier (CFOA). This IC is used in many applications and it can be used in place of traditional op-amps to get much better AC performance and high linearity. The AD844AN is very popular by its applications in current-mode circuits. By using this IC many active current-mode devices can be implemented on a laboratory breadboard like second generation current conveyor (CCII), operational transconductance amplifier (OTA), current differencing buffered amplifier (CDBA), current differencing transconductance amplifier (CDTA) and operational transresistance amplifier (DCCII).

The main advantages of using AD844AN in current-mode applications, the closed-loop bandwidth is independent of the closed-loop gain and free from the slew rate limitations. To investigate the proposed circuits for waveform generation and frequency tuning with respect to the passive components connected to the circuits, the equivalent prototype circuit model of the OTRA shown in Figure 6.2 with two AD844AN ICs is used. For the OTRA prototype circuit ±6 V supply voltages are used to produce the oscillations in all the proposed circuits given in chapter 4.

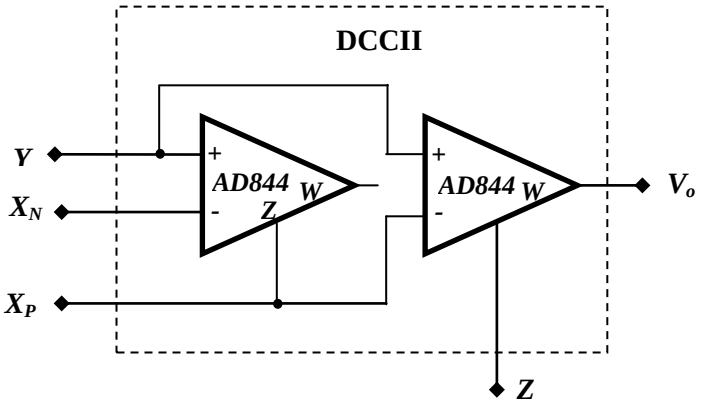


Fig. 6.1. Experimental setup of DCCII using AD844AN.

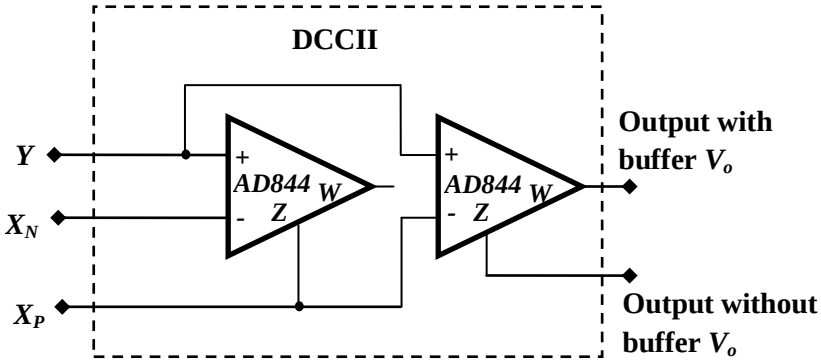


Fig. 6.2. The hardware prototype model of DCCII incorporated using AD844AN.

6.2. Square Waveform Generators Using Single DCCII

6.2.1. Experimental Results

6.2.1.1. Proposed Square Waveform Generator 1

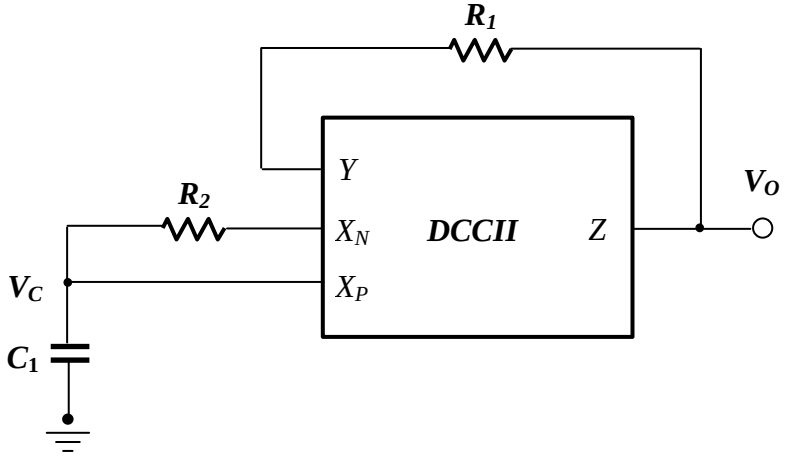


Fig. 6.3. Circuit diagram of proposed square wave generator 1.

The theoretical model of the DCCII can be realized practically by using the commercially available Analog Devices AD844AN. The equivalent model of the DCCII can be achieved by using the two AD844AN ICs. For all the measurements, the supply voltage taken as V_{DD}=-V_{SS}=6 V. By considering the passive components R_1=1 kΩ, R_2=6 kΩ and C=100 nF the operating frequency of 1.01 kHz is achieved.

Figure 6.4 shows the photograph of the oscilloscope output of the proposed square wave generator. In Figure 6.4, the horizontal and vertical scales are 0.5 ms/div and 1 V/div respectively. And from the cadence specre results and Figure 6.4, it has confirmed both experimental and simulated results as well as copes up with the mathematical notation of the time period of the proposed circuit.

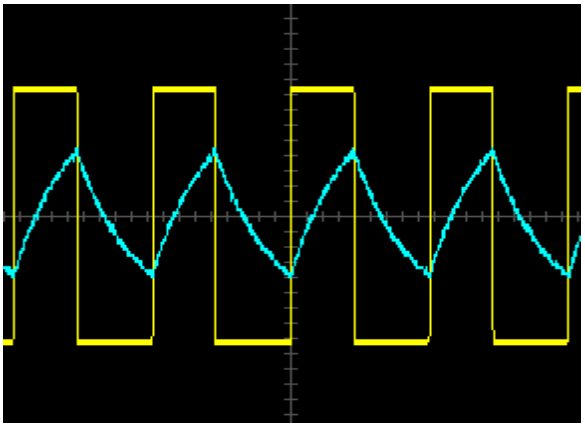


Fig. 6.4. Typical output waveform of circuit shown in Figure 6.3.
Scale: X-axis 0.5 ms/div & Y-axis 1 V/div

6.2.1.2. Proposed Square Waveform Generator 2

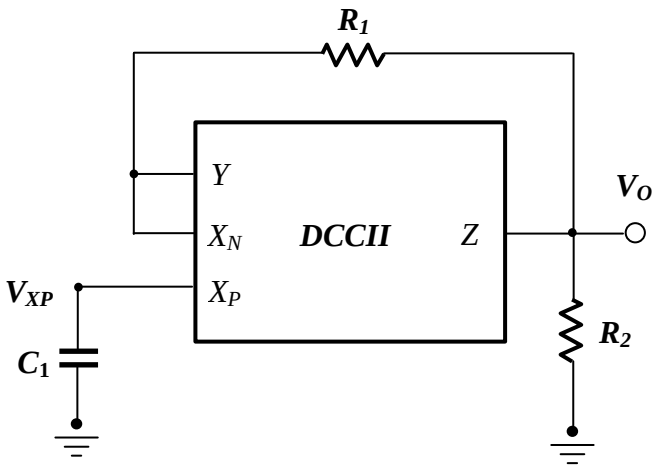


Fig. 6.5. Circuit diagram of proposed square wave generator 2.

A DCCII equivalent model is developed via commercially available current feedback operational amplifiers (CFOA) of AD844AN is shown in Figure 6.1 and the same is tested on laboratory bread board with additionally attached passive components to meet circuit properties. Supply voltage of V_{DD}=–V_{SS}=6 V is considered for hardware setup.

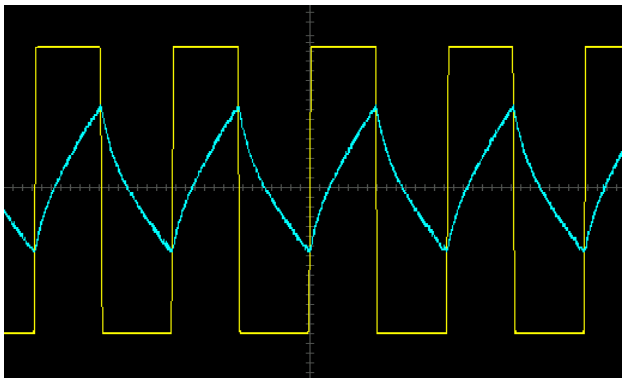


Fig. 6.6. The generated response of circuit shown in Figure 6.5.
Scale: X-axis 0.2 ms/div & Y-axis 2V/div.

The experimental results at the workable frequency range is given in Figure 6.6. The oscilloscope output for proposed circuit with the taken values of R_1 = 5 kΩ, R_2 = 5 kΩ and C = 0.01 μF is shown in Figure 6.6. Both the obtained results of simulated and experimental results in Cadence virtuoso and laboratory setup using AD844AN resemble the identical measures with a satisfying mathematical model of the proposed circuit. And these CFOAs of AD844AN, developed by Analog Devices, have the additional voltage buffer at the output section of the circuitry which has used during the experimental setup. As the graphs obtained from the measured results closely replicated the already presented simulated ones, they are not included here to avoid repetition and for brevity.

6.2.1.3. Proposed Square Waveform Generator 3

The equivalent model of the DCCII is constructed using existing current feedback operational amplifiers (CFOA) of analog devices AD844AN ICs shown in Figure 6.7. The prototype is designed on a laboratory breadboard with the supply voltages of V_{DD} = –V_{SS} = 6 V.

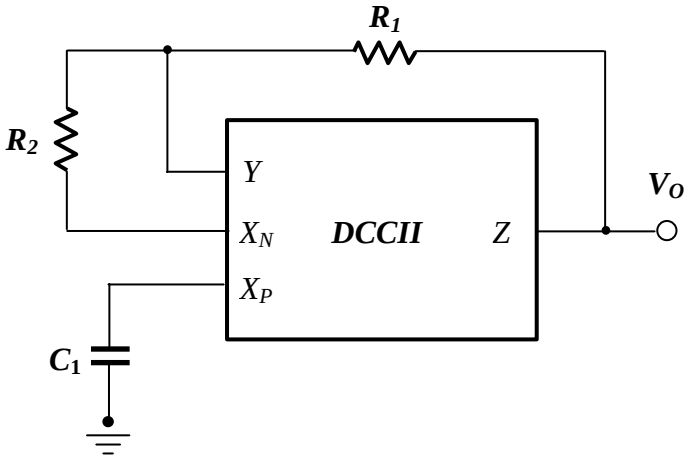


Fig. 6.7. Circuit diagram of proposed square wave generator 3.

The photographic output of the hardware setup is shown in Figure 6.8. The design parameters for the hardware realization are R_1 = 3 kΩ, R_2 = 80 kΩ and C = 0.01 μF, respectively.

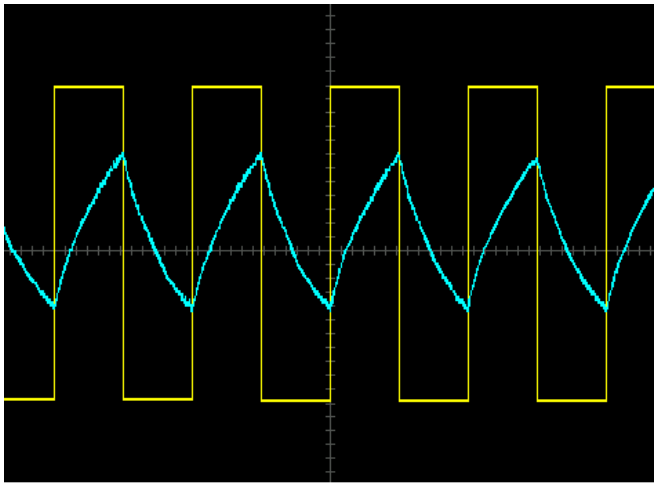


Fig. 6.8. The pictorial view of proposed design using the circuit shown in Figure 6.7. Scale: X-axis 0.2 ms/div & Y-axis 2 V/div.

Compared to that of the existed waveform generator in the literature, the proposed circuit is only has the single active element. And also offers the usage of minimum number of passive components with the provision grounded capacitor feature as it uses metal insulator metal capacitor. This yields negligible amount of parasitics during IC tape out, leads to designer friendly.

6.3. All-pass Filter Circuits

6.3.1. Experimental Results

6.3.1.1. Proposed All-Pass Filter 1

The hypothetical form for the DCCII is developed with the help of commercially available analog devices AD844AN. By using two AD844AN ICs, the equivalent

model of the DCCII can be achieved. The experimental simulation is carried with the supply voltage of V_{DD} = -V_{SS} = 6 V is considered.

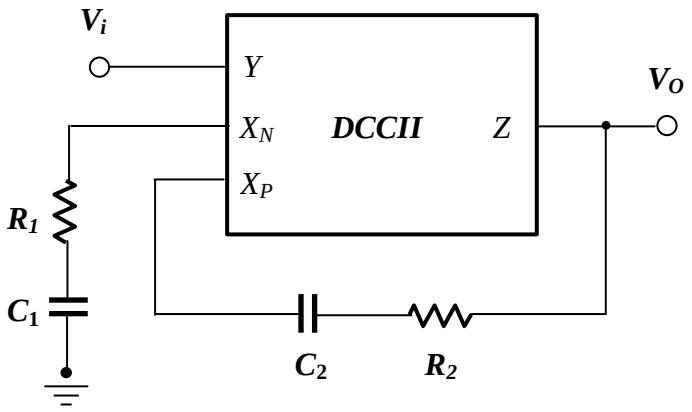


Fig. 6.9. Circuit diagram of proposed All-Pass Filter 1.

The oscilloscope output of the proposed all-pass circuit is shown in Figure 6.10. The scales in the oscilloscope are 0.5 ms/div and 1 V/div for vertical and horizontal labels respectively. Both the simulation and experimental setup results are in good agreement with the theoretical model of the proposed circuit.

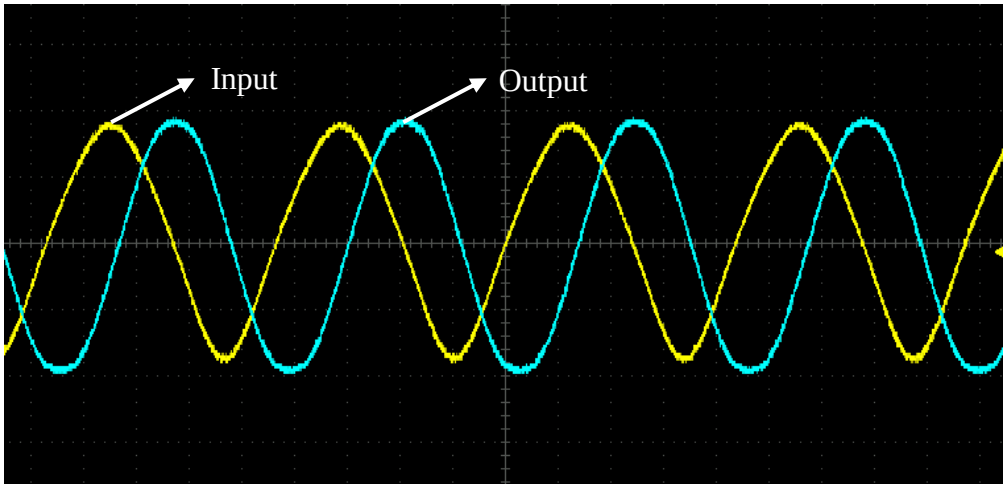


Fig. 6.10. Typical experimental response of circuit revealed in Figure 6.9.
Scale: X-axis 0.5 ms/div & Y-axis 1 V/div

6.3.1.2. Proposed All-Pass Filter 2

The developed all pass filter circuit is experminally verified using the hardware prototype of the DCCII as shown in the Figure 6.11 by additionally joined other discrete passive components. The required potental of V_{DD}=-V_{SS}=6 V is considered for validation.

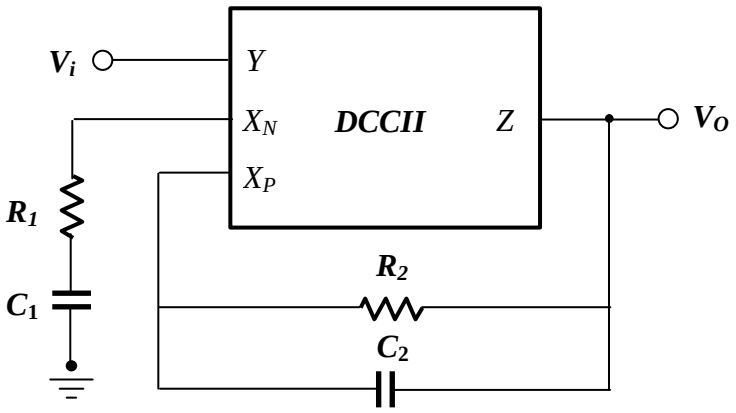


Fig. 6.11. Circuit diagram of proposed All-Pass Filter 2.

The obtained experimental setup output of the proposed circuit depicted in Figure 6.11 is presented in the Figure 6.12. The corresponding scales are given beneath the oscilloscope response. The obtained results of both simulated and experimental results are approximately equal.

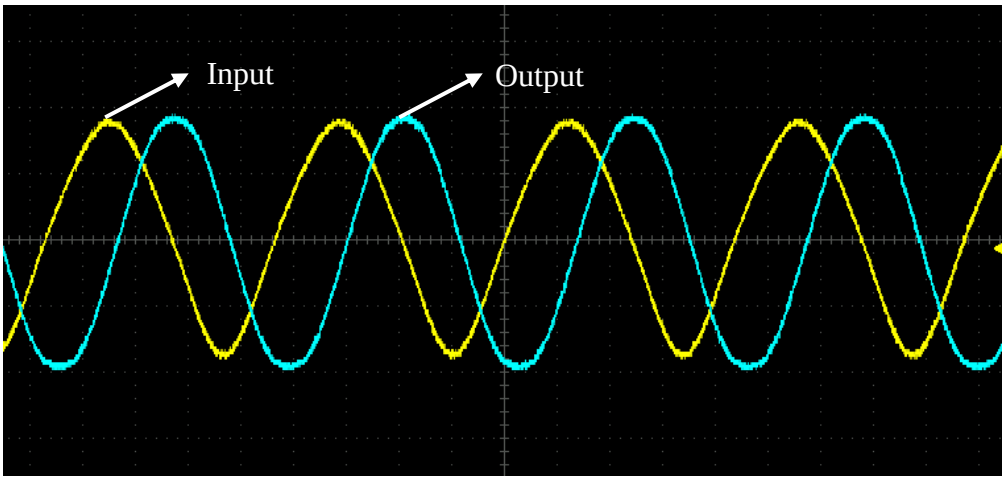


Fig. 6.12. Typical experimental response of the circuit revealed in Figure 6.11.

Scale: X-axis 0.5 ms/div & Y-axis 1 V/div

6.3.1.3. Proposed All-Pass Filter 3

In similar to that of previous methods of verifing the proposed circuits functionality using the experimentally developed hardware equivalent circuit of DCCII, the third proposed all pass filter circuit is tested in the laboratory breadboard with the supply voltages of $V_{DD} = -V_{SS} = 6$ V.

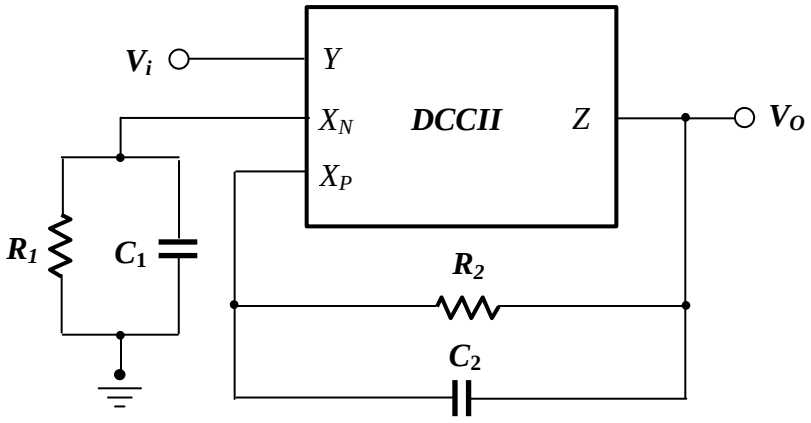


Fig. 6.13. Circuit diagram of proposed All-Pass Filter 3.

The experimental response of the proposed circuit shown in Figure 6.13 is given in the Figure 6.14. The genrated oscillope photograph gives the almost same response as that of simulated graphs and the corresponding hardware result sclales are mentioned as X-axis 0.5 ms/div & Y-axis 1 V/div.

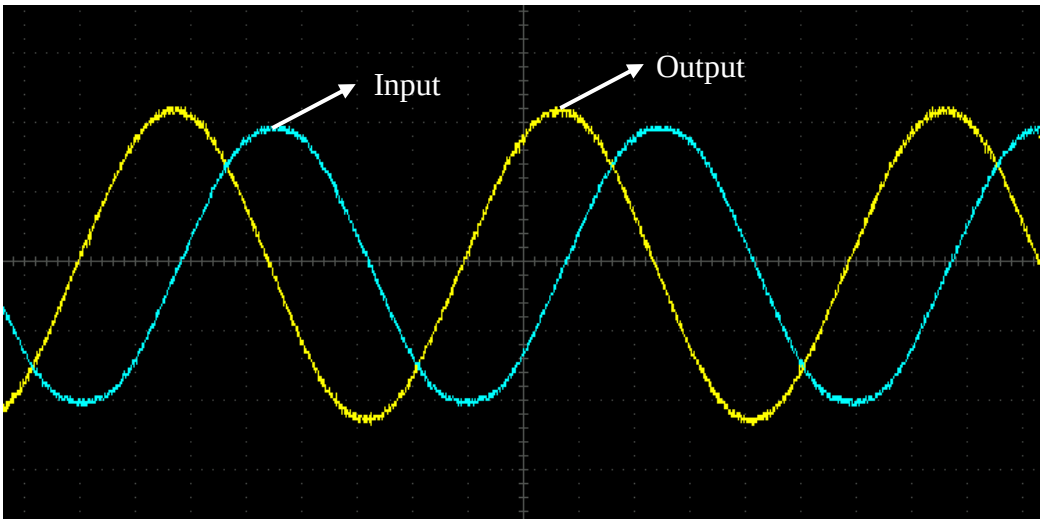


Fig. 6.14. Typical experimental response of the circuit shown in Figure 6.13.
Scale: X-axis 0.5 ms/div & Y-axis 1 V/div

Table 6.1 Comparison of The Proposed Square Wave Generator (Relaxation Oscillator) With The Published Voltage And Current Mode Square Wave Generators

Reference	Device	No. of Active components	No. of passive components	No. of Resistors	No. of Capacitors	Grounded Capacitor	Grounded Resistor	Hardware Implementation
J. M. Jacob et al. [2000]	OpAmp	2	4	3	1	No	No	Yes
B. Almashary et al.[2000]	CCII	2	5	3	2	Yes	Yes	No
AKMS Haque et al. [2008]	CFOA	3	5	4	1	No	Yes	No
Y.K. LO et al. [2007]	OTRA	2	7	4	3	Yes	No	No
A. Sedra et al. [1997]	OTA	3	3	2	1	Yes	No	Yes
J. Kumbun et al.[2010]	MO-CTTA	2	3	2	1	Yes	Yes	No
T. Srisakul et al. [2011]	MO-CCCCTA	2	3	2	1	Yes	Yes	No
Proposed Circuit 3	DCCII	1	3	2	1	Yes	Yes	Yes

Table 6.2 The Details associated with the Proposed Square Wave Generators

Proposed Circuits	No. of Active components	No. of passive components	No. of Resistors	No. of Capacitors	Grounded Capacitor	Maximum Operating Frequency (MHz)	Hardware Implementation
Proposed Circuit 1	2	4	3	1	Yes	1.9	Yes
Proposed Circuit 2	3	3	2	1	Yes	2.2	Yes
Proposed Circuit 3	1	3	2	1	Yes	2.7	Yes

Table 6.3 Comparison of The Proposed all-pass filters With The existing Voltage And Current Mode all-pass filters

Reference	Device	No. of Active components	No. of Transistors	No. of passive components	No. of Resistors	No. of Capacitors	Grounded Capacitor	Hardware Implementation
P. Singthong et al. [2011]	CCCII	3	21	2	0	2	Yes	Yes
K. Pal et al. [2011]	DDCC-	2	44	2	1	1	Yes	Yes
M. A. Ibrahim et al. [2012]	DDCC+	2	24	2	0	2	Yes	Yes
S. Srisakultiew et al. [2012]	CCCII	2	36	4	2	2	Yes	Yes
M. Kumngern et al. [2013]	DDCC	3	21	4	2	2	Yes	No
V. K. Dixit et al. [2014]	DVCC	2	24	2	1	1	No	No
I.A. Khan et al. [2015]	DVCC	2	46	4	2	2	No	No
D. Singh et al. [2015]	MM-CCII	5	23	8	6	2	Yes	Yes
E. Arsalan et al. [2016]	DCCII	1	24	4	3	1	Yes	Yes
Proposed Circuit 4	DCCII	1	21	4	2	2	Yes	Yes

Table 6.4 The Details associated with the Proposed All-Pass Filter Cicuits

Proposed Circuits	No. of Active components	No. of passive components	No. of Resistors	No. of Capacitors	Grounded Capacitor	Hardware Implementation
Proposed Circuit 4	1	4	2	2	Yes	Yes
Proposed Circuit 5	1	4	2	2	Yes	Yes
Proposed Circuit 6	1	4	2	2	Yes	Yes

6.4. Summary

The experimental realization of the proposed circuits using the developed prototype with AD844AN ICs in addition to the externally joined discrete passive components in order to validate the mathematical model and simulation results are carried out in this chapter. The salient features and the core advantages of the introduced models are compared with the existed standard current and voltage mode counterparts and the same are reflected in the tables.

CHAPTER VII

CONCLUSIONS AND SCOPE FOR FUTURE WORK

In this thesis, few models of novel waveform generators and filter circuit designs, operation and synthesis are furnished. The circuits presented in this thesis require reasonably minimum number of active and passive components to generate the waveforms and perform filter applications. The proposed waveform generators and filter circuits are simulated using SPECTRE simulation model parameters and a repetition of them are carried out using commercially available AD844AN ICs on a laboratory breadboard. All the workable and simulated results are correlated in parallel with the theoretical analysis.

7.1. Conclusions

Chapter 1 construes the introductory overview of the importance of square waveform generators and filter circuits in electronic circuits and the evolution of active devices in waveform generation from voltage mode to the current mode. This chapter also covers the advantages derived by the current mode devices over voltage mode devices.

In chapter 2, the main active device used for the design and implementation of waveform generators are given. The CMOS implementations of the DCCIIs given in (K.N. Salama et al, 1999, A. Toker et al, 2000) are used for waveform generation. The CMOS DCCII structures are redesigned using Cadence CMOS gpdk 180 nm technology and simulated using SPECTRE simulation model parameters. The CMOS transistors W/L ratios are also given. In order to validate the proposed circuits, the OTRA is implemented on the laboratory breadboard by using commercially available ICs AD844AN. The implementation of OTRA using two AD844AN ICs and a resistor are covered in this chapter.

The main emphasis of Chapter 3 is on existing applications. And, waveform generators are designed using DCCII. This chapter also provides the analysis and important issues involved in the design and implementation of the various applications by using DCCII in detail. Each sub-section related to the applications of DCCII also

provides advantages and disadvantages of the available DCCII based waveform generators in the literature.

Chapter 4-6 presents the main objective of the thesis. Novel active filters and square waveform generators are designed in chapter 4. The operation of the proposed waveform generators is discussed in this chapter. Some special case oscillator circuits by using the single DCCII are presented in this chapter. In these waveform generator circuits, all the proposed circuits are having a single grounded capacitor circuit. In all the proposed circuits, in order to realize a voltage controlled oscillator, the grounded resistance/capacitance can be replaced by a JFET. This square waveform generates a fixed and almost equal on-duty and off-duty cycles. The time period of the output waveform can be varied by any of the passive components that are connected to the circuit. The designed circuits make a linear variation of the time period with respect to the passive components connected to in the circuit. The square waveform generator circuits conferred in this chapter will be able to vary both the on-duty and off-duty cycles at a time. These circuits are designed with one DCCII, two resistors and a single capacitor. By varying the passive component values, the on-duty and off-duty cycles can be adjusted to the required time period. The operation of the square waveform generators to oscillate between the positive saturation to the negative saturation levels is depicted in this chapter. In chapter 4, the mathematical derivations for each circuit are presented. The mathematical model for the frequency of operation is derived by applying the general network laws to the circuits. By considering the ideal behavior of the DCCII, the mathematical derivation for the time period of the proposed square waveform generators is carried.

In chapter 5, the simulation results for the newly proposed circuits in chapter 4 are given. All the proposed circuits are designed with the CMOS DCCII realization given in chapter 2 along with a few passive components. The proposed circuits in chapter 4 are simulated using SPECTRE simulation model parameters with a supply voltage of ± 2.5 V. The simulated output waveforms of the proposed circuits along with passive component values are used to validate the theoretical analysis. The simulated results are in good agreement with the mathematical analysis given in the previous chapter. Some new square waveform generators are proposed in chapter 4. These circuits have the fixed duty cycle square waveform generator i.e. the on-duty and off-duty cycles are fixed and almost equal with this circuit and are able to vary the

duty cycles to the required time period. For producing the square waveform in the proposed square waveform generators, the required time period is to be chosen first. Then the passive component values are arbitrarily determined from the time period equation derived in chapter 4. The capacitor and resistance values can be tuned accordingly to select the required time period or frequency. These square waveform generators are also called as a variable duty cycle waveform generators. In these waveform generators the resistance values are chosen to select the on-duty cycle time period which is than the off-duty cycle time period. If the off-duty cycle time period is greater than the on-duty cycle time period, the resistance values will be reversed. The simulated output waveforms are matched well with the theoretical analysis given in the previous chapter.

This chapter aims at the workability of the new topologies proposed in chapter 4. All the circuits presented in this thesis are experimentally scrutinized for waveform generation using laboratory breadboard. The prototype DCCII realization using two AD844AN ICs shown in chapter 2 is used to validate the theoretical and simulation analysis with the hardware results. The IC AD844AN is a high speed monolithic current feed-back operational amplifier. This IC is very popular by its applications in current-mode circuits. The oscillator circuits generated from the generalized configuration are connected on the laboratory breadboard for testing the waveform generation and frequency tuning.

The passive components that are used for generating sinusoidal oscillations and frequency tuning are used to validate the theoretical analysis. A supply voltage of ± 6 V is used for all the measurements that are to be done on laboratory breadboard. The photographic pictures of the output waveforms on the oscilloscope screen are shown in this chapter. The percentage of error between the theoretical frequencies and experimental frequencies of the proposed circuits are represented. The proposed circuits have the advantage of tuning independently with respect to the passive component.

The frequency tuning of these circuits is presented in the form of figures. For frequency tuning, one of the passive components connected to the circuit is varied over a range while the other passive components are kept to be constant. The comparison of the proposed waveform generator circuits realized from the literature in terms of number of active and passive components, supply voltage and power

consumption to produce the waveform are presented in this chapter. Similarly, the filter circuits are also implemented and checked for waveform generation using a laboratory breadboard. The output waveform in the oscilloscope and frequency tuning with respect to the passive components are presented in the form of plots.

The required time period is chosen first, for generating the square waveform in the square waveform generators that are proposed in chapter 4. Then the passive component values are to be calculated from the time period equation shown in chapter 5. The experimental output waveforms of the square waveform generators are shown to validate the mathematical analysis and to carry out the simulation analysis. The time period tuning with respect to the passive components is presented in the form of plots. From these plots, the time period curve is observed to be more linear than the existing DCCII based square waveform generator. The comparison of the proposed square waveform generator with the conventional DCCII based square waveform generator is given in terms of number of active components, number of passive components, impedance level, grounded components to produce the square waveform.

7.2. Scope For Future Work

Further work can be done by implementing the DCCII in sub-microvolt region to decrease the supply voltage and power consumption. The DCII can be implemented using FinFET, TFET, HTFET and CNTFET to achieve the low power consumption with low supply voltage. And based on these versatile features of high frequency and slew rate the proposed circuits can be used for instrumentation amplifier circuits in the biomedical applications.

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