18MC106COMPUTER ORGANIZATION

Course Description and Objectives:

This course introduces Register Transfer Language, Computer Arithmetic, Basic Computer Organization and Design, Pipeline processing, Memory and Input/Output Organizations. Further, it helps to understand and analyze the functional organization of a digital computer. The objective of the course is to enable the students to understand the basic structure and operation of a digital computer and also to know in detail the operation of the arithmetic unit, logical unit, control unit and the different ways of communicating with I/O devices. It also helps a student to learn the hierarchical memory organization and interfacing.

Course Outcomes:

The student will be able to:

- Demonstrate and understand the basic principles and operations of digital computers.
- Evaluate the design issues of digital computer systems including arithmetic logic unit, control unit, communication with peripheral devices and interrupt handling.
- Develop pipeline architectures for RISC processors.
- Differentiate the various memory and I/O interfaces.

Skills:

- Perform fixed and floating point arithmetic operations.
- Identifying the types of memories and their time complexities.
- Perform I/O data transfer in serial and parallel modes.

Activities:

- Simulate arithmetic, logic and shift operations.
- Case Studies on various types of memories used in I3, I5 and I7 processors.
- Preparation of a report on RISC processors used in mobile phones.

Syllabus

UNIT – 1 **12 Hours**

INTRODUCTION & RTL: Organization and architecture, Block diagram of digital computer, Structure and function; Register transfer language – Register transfer bus and memory transfers.

UNIT – 2 **12 Hours**

COMPUTER ARITHMETIC: Arithmetic micro-operations, Logic micro-operations, Shift micro-operations and Arithmetic Logic Shift unit; Addition, subtraction, Multiplication and Division algorithms, Floating point representation and its operations.

UNIT – 3 **12 Hours**

BASIC COMPUTER ORGANIZATION AND DESIGN: Instruction codes, Computer registers, Computer instructions, Instruction cycle, Memory–Reference instructions, Register reference instructions, Input-Output and Interrupt, Stack organization, Instruction formats, Addressing modes, Data transfer and manipulation, Program control, Reduced Instruction Set Computer.

UNIT – 4 **12 Hours**

PIPELINE PROCESSING & MEMORY ORGANIZATION: Pipeline processing-Parallel processing, Pipelining, Arithmetic pipeline, Instruction pipeline, RISC pipeline; The memory organization – Memory Hierarchy, Main memory, Auxiliary memory, Associative memory, Cache memory, Virtual memory**.**

UNIT – 5 **12 Hours**

INPUT-OUTPUT ORGANIZATION: Peripheral devices, I/O interface, Asynchronous data transfer, Modes of transfer, Priority interrupt, Direct Memory Access, Input-Output Processor (IOP), Serial communication.

Text Books:

1. M.Moris Mano, "Computer Systems Architecture", 3rd edition, Pearson/Prentice Hall India, 2007.
2. William Stallings, "Computer Organization and Architecture", 7th edition, Pearson/Prentice Hall India , 2007.

Reference Books:

1. Carl Hamacher, ZvonkoVranesic and SafwatZaky, "Computer Organization", 5th edition, Tata McGraw Hill, 2007.
2. Vincent P. Heuring and Harry F Jordan, "Computer Systems Design and Architecture", 2nd edition, Pearson/Prentice Hall India, 2004.
3. David A Patterson and John L Hennessy, "Computer Organization and Design - The Hardware/Software Interface, ARM edition", 5th edition, Elsevier, 2009.