17VL017 ADVANCED DIGITAL SYSTEMS DESIGN

Hours Per Week :

L	T	P	C
3	1	-	4

Total Hours :

L	T	P
45	15	-

WA/RA	SSH/HSH	CS	SA	S	BS
15	30	-	5	5	-

Course Objectives:

- The objective of this course is to study methods to design of synchronous and asynchronous sequential circuits. This course also introduces testing algorithm techniques for combinational circuits, sequential circuits and PLAs & minimization and folding techniques of PLAs.

Course Outcomes:

Upon successful completion of this course student should be able to:

- Ability to analyze and design synchronous and asynchronous sequential circuits.
- Ability to understand the testing of combinational, sequential and PLAs.
- Ability to understand the PLA folding and minimization.

SKILLS:

- Students able to learn the various digital systems and technologies include FPGA's.
- Students able to find how to test the digital circuit and what are different types of faults and how to eliminate those faults.

UNIT - I

SYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN & ASM CHARTS : Reduction of State Tables State Assignments,Sequential Circuit Design:- Design of Code Converter,Design of Iterative Circuits.Design of Sequential Circuits Using ROMs and PLAs, Sequential Circuit Design using CPLDs and FPGAs. ASM Charts.

UNIT - II

FAULTS IN DIGITAL CIRCUITS & TEST GENERATION FOR COMBINATIONAL CIRCUITS : Faults in Digital Circuits:-Failures and Faults, Modelling of Faults, Temporary Faults. Test Generation for Combinational Circuits:- Fault Diagnosis of Digital Circuits, Path Sensitization Technique, Boolean Difference Method, D-Algorithm, PODEM Algorithm, FAN, Delay Fault Detection. Detection of Multiple Faults.

UNIT - III

STATE-IDENTIFICATION EXPERIMENTS AND TESTING OF SEQUENTIAL CIRCUITS : Experiments, Homing Experiments,Distinguishing Experiments, Machine Identification, Checking Experiments, Design of Diagnosable Machines, Alternative Approaches to the Testing of Sequential Circuits, Design for Testability, Built-In Self-Test (BIST).

UNIT - IV

PROGRAMMABLE LOGIC ARRAYS : PLA Minimization and PLA Folding-The Compact Algorithm, Practical PLA s. PLA testing – Fault in PLA, Test Generation, DFT Schemes, Built-In Self Test.

UNIT - V

ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN : Analysis of Asynchronous Sequential Circuit (ASC) – Fundamental Mode Model, Flow Table, State Reduction, Design of ASC. Hazards, Races and Cycles.

TEXT BOOKS

1. Charles H. Roth Jr. and Larry L. Kinney, “Fundamentals of Logic design”, 6th ed.,Thomson Learning, 2004.
2. Parag K Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.
3. Zvi Kohavi and Niraj K.Jha, “Switching and Finite Automata Theory”,3rd., Cambridge University Press, 2010.
4. Nripendra N Biswas, “Logic Design Theory”, Prentice Hall of India, 2001.
5. John M Yarbrough, “Digital Logic applications and Design”, Thomson Learning, 2001.

REFERENCE BOOKS

1. Donald G. Givone, “Digital principles and Design”, Tata McGraw Hill 2002.
2. Stephen Brown and Zvonk Vranesic, “Fundamentals of Digital Logic with VHDLDeisgn”, Tata McGraw Hill, 2002.
3. Mark Zwolinski, “Digital System Design with VHDL”, Pearson Education, 2004.

ACTIVITIES:

- Design an ALU using PLA.
- Algorithm for fault finding in sequential circuits.
- Students able to perform the experiment on FPGA’s (Spartan 3E,vertex) boards.
- Students able to design the testing circuits by using testing methods (BIST).