17VL016 SEMICONDUCTOR MEMORY DESIGN

Hours Per Week :

L	T	P	C
4	-	-	4

Total Hours :

L	T	P
60	-	-

WA/RA	SSH/HSH	CS	SA	S	BS
15	30	-	5	5	-

Course Objectives:

To acquire knowledge about different types of semiconductormemories.

- To study about architecture and operations of different semiconductor memories.
- To comprehend the low power design techniques andmethodologies.

Course Outcomes:

Analysis the different types of RAM, ROM designs.

- Analysis the different RAM and ROM architecture and interconnects.
- Analysis about design and characterization technique.
- Analysis of different memory testing and design for testability.
- Identification of new developments in semiconductor memorydesign.

SKILLS:

- In-depth understanding of volatile and nonvolatile SRAMs, DRAMs.
  Analyse and test the advanced memory designs.

UNIT - I

Random Access Memory Technologies: Static Random Access Memories(SRAMs):SRAM cell structure- MOS SRAM architecture, MOS SRAM cell andperipheral circuit operation, bipolar SRAM technologies, silicon on insulator(SOI) technology, advanced SRAM architectures and technologies, applicationspecific SRAMs.

Dynamic Random Access Memories (DRAMs): DRAM technology development, CMOS CRAMs, DRAMs cell theory and advanced cell structures-BiCMOS DRAMs-soft error failure in DRAMs, Advanced DRAM designs andarchitecture, application specific DRAMs.

UNIT – II

Nonvolatile Memories: Masked Read, only memories (ROMs): High densityROMs, programmable read-only memories (PROMs)- bipolar PROMs, CMOSPROMs, erasable (UV)- Programmble read-only memories (EPROMs)-Floating Gate EPROM cell- one, time progammable (OTP) Eproms ElectricallyErasable PROMs (EEPROMs), EEPROM technology and architecture,nonvolatile SRAM-Flash memories (EPROMs or EEPROM), Advanced flashmemory architecture.

UNIT – III

Memory fault modeling, testing and memory design for Testability andfault tolerance, RAM fault modeling, electrical testing, Peusdo randomtesting, megabit DRAM testing nonvolatile memory modeling and testing,IDDQ fault modeling and testing, application specific memory testing.

UNIT – IV

Semiconductor memory reliability and radiation effects: General Reliability issues, RAM failure modes and mechanism, nonvolatile memory reliability,reliability modeling and failure rate prediction, design for reliability, reliability test structures, reliability screening and qualification.

Radiation effects, single event phenomenon (SEP)- radiation hardeningtechniques, radiation hardening process and design issues, radiation hardened memory characteristics, radiation hardness assurance and testing,radiation dosimetry, water level radiation testing and test structures.

UNIT – V

Advanced memory technologies and high-density memory packaging technologies:Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs)FRAMs, Analog memories magnetoresistive random access memories(MRAMs), Experimental memory devices.

Memory hybrids and MCMs (2D), Memory stacks and MCMs (3D), Memory MCM testing and reliability issues- memory cards- high density memory packaging future directions.

ACTIVITIES:

- Design of 6T SRAM, 7T SRAM, DRAM circuits
- Design of Sensing Amplifiers

TEXT BOOKS

1. Ashok K.Sharma, Semiconductor Memories Technology, testing andreliability, Prentice hall of India Private Limited, New Delhi 1997.
2. Ashok K Sharna, Advanced Semiconductor Memories – Architecture, Designand Applications, Wiley 2002.

REFERENCE BOOKS

1. Anjan Ghosh, High Speed Semiconductor Devices, NPTEL Courseware,2009.