17VL015 CAD VLSI

Hours Per Week :

L	T	P	C
3	1	-	4

Total Hours :

L	T	P
45	15	-

WA/RA	SSH/HSH	CS	SA	S	BS
15	30	-	5	5	-

Course Objectives:

- To provide an introduction to the fundamentals of Computer-Aided Design tools for the modeling, design, analysis, test, and verification of digital Very Large Scale Integration (VLSI) systems. · To learn Physical design of VLSI Circuits ·
- To learn the Basics of Graph Theory Algorithms ·
- To understand the concept of CAD Tools. · To Learn the Physical Design of FPGA and MCMS

Course Outcomes:

Upon successful completion of this course student should be able to:

- Demonstrate knowledge and understanding of fundamental concepts in CAD.
- Demonstrate knowledge of computational and optimization algorithms and tools applicable to solving CAD related problems.
- Establish capability for CAD tool development and enhancement.
- Get the Overview of Physical Design of VLSI ICs .
- Gain the Knowledge of Graph Theory.
- Able to Design Backend Process using CAD Tools.
- To Get the Knowledge about Physical design of FPGA and MCMS.

SKILLS:

- Able to perform circuit extraction and simulation.
- Able to develop physical layout design.
- Able to perform logic verification.

UNIT – I

Introduction to VLSI Design Automation Introduction to VLSI Methodologies - VLSI Physical Design Automation - Design and Fabrication of VLSI Devices - Fabrication process and its impact on Physical Design.

UNIT – II

Graph Theory A Quick Tour of VLSI Design Automation Tools - Data structures and Basic Algorithms- Algorithmic Graph theory and computational complexity - Tractable and Intractable problems.

UNIT – III

CAD Tools General purpose methods for combinational optimization - partitioning - floor planning and pin assignment - placement - routing.

UNIT – IV

Simulation and Synthesis Simulation-logic synthesis -Verification-High level synthesis-Layout synthesis- Compaction.

UNIT – V

Design Automation of FPGA and MCMS Physical Design Automation of FPGAs, MCMS-VHDL-Verilog-Implementation of Simple circuits using VHDL and Verilog.

TEXT BOOKS

1. N.A. Sherwani, " Algorithms for VLSI Physical Design Automation ", 1999. 2. S.H.Gerez, " Algorithms for VLSI Design Automation", 1998.
2. Wayne Wolf "Modern VLSI Design",Third edition.
3. S.Smith "Application Specific Integrated Circuits". 5. S. Y. Kung, H. J. Whilo House, T.Kailath, " VLSI and Modern Signal Processing Prentice Hall, 1985.

REFERENCE BOOKS

1. Jose E. France, YannisTsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.

ACTIVITIES:

- Design and testing of half adder /full adder.
- Design and testing of 8 bit ALU.
- Design a 6 transistor memory cell.
- Design of dynamic logic d nand, d nor and d xor.