17VL008 MODELLING AND SYNTHESIS WITH VERILOG HDL

Hours Per Week :

L	T	P	C
3	-	3	5

Total Hours :

L	T	P
45	-	45

WA/RA	SSH/HSH	CS	SA	S	BS
15	30	-	5	5	-

Course Objectives:

- To design combinational, sequential circuits using Verilog HDL.
- To understand behavioral and RTL modeling of digital circuits.
- To verify that a design meets its timing constraints, both manually and through the use of computer aided design tools.
- To simulate, synthesize, and program their designs on a development board.
- To verify and design the digital circuit by means of Computer Aided Engineering tools.which involves in programming with the help of Verilog HDL.

Course Outcomes:

Upon successful completion of this course student should be able to:

- Understand the basic concepts of verilog HDL
- Model digital systems in verilog HDL at different levels of abstraction
- Know the simulation techniques and test bench creation.
- Understand the design flow from simulation to synthesizable version
- Get an idea of the process of synthesis and post-synthesis

SKILLS:

- Able to design digital circuit by HDL.
- Able to realize digital circuit on FPGA kits

ACTIVITIES:

- Write a program for 8 bit addition by using different data types.
- Write a program for 8x1 multiplexer
- Write a program for D flip flop.
- Write a program for shift register.
- Write a program for ALU

UNIT - I

Hardware modeling with the verilog HDL. Encapsulation, modeling primitives, different types of description.

UNIT - II

Logic system, data types and operators for modeling in verilog HDL. Verilog Models of propagation delay and net delay path delays and simulation, inertial delay effects and pulse rejection.

UNIT - III

Behavioral descriptions in verilog HDL - Verilog behaviors, behavioral statements, procedural assignments, procedural continuous assignments, timing controls and synchronization, blocking and non blocking assignments, constructs for activity flow control, tasks and functions, behavioral models of FSM.

UNIT - IV

Synthesis of combinational logic: HDL-based synthesis - technology-independent design, styles for synthesis of combinational and sequential logic, synthesis of finite state machines, synthesis of gated clocks, design partitions and hierarchical structures.

UNIT - V

Synthesis of language constructs, nets, register variables, expressions and operators, assignments and compiler directives. Switch-level models in verilog. Design examples in verilog.

Modelling and Synthesis with Verilog HDL Lab

List of Experiments:

1. Design of combinational circuits using EDA Tools.
2. Design of sequential circuits using EDA Tools.
3. Design of 4-bit binary, BCD counters using EDA Tools (synchronous/ asynchronous reset).
4. Design of a N- bit Register using EDA Tools.
5. Design of Sequence Detector using EDA Tools (Finite State Machine- Mealy and Moore Machines).
6. Design of 4- Bit Multiplier, Divider using EDA Tools.
7. Design of ALU using EDA Tools.
8. Serial adder.
9. Memories.
10. Implement Real time small application digital circuit on FPGA - Case study.

TEXTBOOKS:

1. M.D.Ciletti, “Modeling, Synthesis and Rapid Prototyping with the Verilog HDL”, PHI, 1999.
2. S. Palnitkar, “Verilog HDL – A Guide to Digital Design and Synthesis”, Pearson, 2003.

REFERENCE BOOKS:

1. J Bhaskar, “A Verilog HDL Primer (3/e)”, Kluwer, 2005
2. M.G.Arnold, “Verilog Digital – Computer Design”, Prentice Hall (PTR), 1999.
3. Recent literature in Modeling and Synthesis with Verilog HDL.