17VL005 VLSI TECHNOLOGY

Hours Per Week :

L	T	P	C
4	-	-	4

Total Hours :

L	T	P
60	-	-

WA/RA	SSH/HSH	CS	SA	S	BS
15	30	-	5	5	-

Course Objectives:

- To understand the Fabrication of ICs and purification of Silicon in different technologies.
- To impart in-depth knowledge about Etching and deposition of different layers.
- To understand the different packaging techniques of VLSI devices.

Course Outcomes:

Upon successful completion of this course student should be able to:

- The ability to use metallization techniques to create three dimensional device structures and devices.
- The ability to know methodology to fabricate an IC's.

SKILLS:

- Ability to apply knowledge on different fabrication steps and design of different technology circuits using MOSFETS.
- Ability to utilize a System approach to design a chip and operational performance.

UNIT – I

Crystal Growth, Wafer Preparation, Epitaxy and Oxidation : Metallurgical Grade Silicon, Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, Etching, Polishing, Chemical Cleaning, gettering treatment, Vapor phase Epitaxy, Epitaxial Evaluation, Growth Mechanism, Introduction to Oxidation Techniques.

UNIT – II

Lithography, Deposition,Diffusion and Ion Implantation : Optical Lithography, Electron Lithography, Deposition process, CVD, Poly-silicon, structure, properties of Silicon Dioxide, Annealing, Furnace Annealing.

UNIT – III

Metallization, VLSI Process Integration and Packaging : Physical Vapor Deposition (PVD), NMOS IC Technology, CMOS IC Technology, BICMOS IC Technology, Packaging, packaging types and Packaging Design Considerations.

UNIT – IV

Introduction to MOS Technology and Electrical Properties : Introduction to MOS technology, Basic MOS transistors, MOS transistor operation, Drain current Vs voltage derivation, MOS Transistor parameters: threshold Voltage, gm, gds, pass transistor, NMOS inverter, Various Pull ups, Determination of pull up to pull down ratio for an NMOS inverter, CMOS inverter, DC Characteristics, Bi-CMOS inverter, Latch up in CMOS circuits.

UNIT – V

VLSI Circuit Design Processes and Circuit concepts and characterization : VLSI Design Flow, MOS Layers, Stick diagrams, Design rules, Layout generation- nMOS, CMOS, Bi-CMOS, Sheet Resistance, Standard unit of capacitance, Delay estimation, Power dissipation, Interconnect, Design margin, Scaling.

ACTIVITIES:

- *Very Fast and Low Power Carry Select Adder Circuit using cadence tool.*
- *Layout generation.*

TEXT BOOKS:

1. S.M.Sze, *VLSI Technology*, 2nd edition, McGraw Hill, 2003.
2. Kamran Eshraghian, Eshraghian Dougles and A. Pucknell, Essentials of VLSI circuits and systems, 1st Edition. PHI, 2005.

REFERENCE BOOKS:

1. Amar Mukherjee, *Introduction to NMOS and CMOS VLSI System Design*, 1st edition, PHI, 2000.
2. James D Plummer, Michael D. Deal and Peter B. Griffin, *Silicon VLSI Technology: Fundamentals Practice and Modeling*, 1st edition, PHI, 2000.
3. Wai Kai Chen, *VLSI Technology*, 1st edition,CRC press, 2003.
4. Rainer Waser *,Nano Electronics and Information Technology ,* Wiley VCH – April 2003. AND *.S.K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc., New York, 2nd edition, 1983.*
5. Nandita Das Gupta, *VLSI technology,* NPTEL Courseware.
6. Neil H.E.Weste and D.M.Harris, CMOS VLSI Design, Third Edition, PEARSON, 2011