17VL004 VLSI TESTING AND VALIDATION

Hours Per Week :

L	T	P	C
4	-	-	4

Total Hours :

L	T	P	WA/RA	SSH/HSH	CS	SA	S	BS
60	-	-	15	30	-	5	5	-

Course Objectives:

- To involve the students in the theory and practice of VLSI test and validations.
- To introduce advanced techniques for efficiently testing and validating the VLSI design.
- To introduce the concept of Design for Test and the technique of automated test pattern generation.

Course Outcomes:

Upon successful completion of this course student should be able to:

- Effectively test VLSI systems using existing test methodologies, equipments, and tools.
- Define a methodology to test the combinational and sequential circuits.
- To construct a Design for Testability (DFT) algorithm for VLSI Circuits.

SKILLS:

- Able to implement DFT techniques for VLSI Circuits
- Able to design any testable combinational logic circuit.
- Able to identify and analyse the yield of chips.

ACTIVITIES:

- How to detect the presence of fault in a circuit using different simulator techniques.
- Find a test vector for the circuit that stucks at 1 faults using combinational and sequential circuits.
- Find a device faults by using IDDQ technique.
- How to scan a by using system level approaches.
- How to test a memory by test algorithm.

UNIT – I

Introduction to VLSI Testing

Introduction - VLSI Testing Process And Test Equipment - Test Economics And Product Quality – Fault Molding-Logic And Fault Simulation.

UNIT – II

Test Generation for Combinational and Sequential Circuits Test generation for combinational logic circuits - Testable combinational logic circuit design - Test generation for sequential circuits - design of testable sequential circuits

UNIT – III

Advanced Testing Memory Test- Memory Density and Defect Trends, Faults **MEMORY TEST** Delay Test- IDDQ Test

UNIT – IV

Design for Testability : Design for Testability - Ad-hoc design - Storage cells for scan designs - Generic scan based design - System level DFT approaches

UNIT – V

Self Test and Test Algorithms : Built-In Self Test - Test pattern generation for BIST - Circular BIST – BIST Architectures - Testable Memory Design - Test algorithms - Test generation for Embedded RAMs.

TEXT BOOKS:

1. Viswani D.Agarval Michael L.Bushnell, “Essentials of Electronic Testing forDigitalMemory & Mixed Signal VLSI Circuit “, Kluwer Academic Publications, 2000.
2. L. T. Wang, C. W. Wu, and X. Wen, VLSI Test Principles and Architectures, Morgan

REFERENCE BOOKS:

1. Kaufmann Morgan Kaufmann Publishers, 2006 M. Abramovici, M.A. Breuer and A.D. Friedman, “Digital Systems and Testable Design”, Jaico Publishing House, 2002.
2. Alfred L.Crouch “Design for Test for Digital IC’s And Embedded Core Systems “, -PHI 1999