17ES016 COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

Hours Per Week :

L	T	P	C
3	1	-	4

Total Hours :

L	T	P
45	15	-

WA/RA	SSH/HSH	CS	SA	S	BS
15	30	-	5	5	-

Course Objectives:

Includes the organization and architecture of computer systems hardware; instruction set architectures; addressing modes; register transfer notation; processor design and computer arithmetic; memory systems; hardware implementations of virtual memory, and input/output control and devices. This course covers the architecture and enabling technologies of parallel and distributed computing systems and their innovative applications. To understand the concepts of computer architecture. To understand the concepts of pipelined and parallel processing.

Course Outcomes:

- Describe the principles of computer design
- Describe the operation of performance enhancements such as pipelines, dynamic scheduling, branch prediction, caches, and vector processors.
- Describe modern architectures such as Super Scalar, vector processors .
- Develop applications for high performance computing systems.

SKILLS:

- Understand the design and architectures of different systems
- Understand the concept of parallel processing

ACTIVITIES:

- *Design and Develop the architectures of different systems.*
- *Design of SIMD*

UNIT - I

Theory of Parallelism Parallel Computer models – the state of computing, Multiprocessors and Multicomputers and Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks, Program and network properties – Conditions of parallelism.

UNIT - II

Partitioning and Scheduling Program partitioning and scheduling, Program flow mechanisms, System interconnect architectures, Principles of scalable performance – performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.

UNIT - III

Hardware Technologies Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory – backplane bus systems, cache memory organizations, shared memory organizations, sequential and weak consistency models.

UNIT - IV

Pipelining and Superscalar Technologies Parallel and scalable architectures, Multiprocessor and Multicomputers, Multivector and SIMD computers, Scalable, Multithreaded and data flow architectures.

UNIT - V

Software and Parallel Processing Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.

TEXT BOOKS:

1. Kai Hwang “Advanced Computer Architecture”. McGraw Hill International 2001
2. Carl Homacher, Zvonko Vranesic, Sefwat Zaky, “Computer Organisation”, 5th Edition, TMH, 2002.

REFERENCE BOOKS:

1. Dezso Sima, Terence Fountain, Peter Kacsuk, “Advanced computer Architecture – A design Space Approach”. Pearson Education,2003.
2. David E. Culler, Jaswinder Pal Singh with Anoop Gupta “Parallel Computer Architecture” ,Elsevier, 2004.
3. John P. Shen. “Modern processor design Fundamentals of super scalar processors”, Tata McGraw Hill 2003.
4. Sajjan G. Shiva “Advanced Computer Architecture”, Taylor & Francis, 2008.