(EC538) VLSI SIGNAL PROCESSING
(ELECTIVE - II)

Objective of the Course :

This course covers techniques for designing efficient DSP architectures. The objective is to realize architectures that will process high throughout data end/or require less power and / or less chip area.

UNIT- I

Introduction to DSP systems - Iteration Bound - Pipelined and parallel processing.
Unit

UNIT- II

Retiming - Unfolding - Algorithmic strength reduction in filters and transforms.Systolic architecture design - fast convolution - Pipelined and parallel recursive and adaptive filters.

UNIT- III

Systolic architecture design - fast convolution - Pipelined and parallel recursive and adaptive filters..

UNIT- IV

Scaling and round off noise - Digital lattice filter structures - Bit level arithmetic architecture - Redundant arithmetic.

UNIT- V

Numerical strength reduction - Synchronous, wave and asynchronous pipe lines - low power design -programmable digital signal processors.

Text Books:

1. *Keshab K.Parthi, " VLSI Digital Signal Processing systems, Design and implementation ",Wiley, Inter Science, 1999.*

References:

1. *Mohammed Isamail and Terri Fiez, "Analog VLSI Signal and Information Processing ", Mc Graw-Hill, 1994.*
2. *S.Y. Kung, H.J. White House, T. Kailath, " VLSI and Modern Signal Processing ", Prentice Hall, 1985.*
3. *Jose E. France, Yannis Tsividis, " Design of Analog - Digital VLSI Circuits for Telecommunication and Signal Processing ", Prentice Hall, 1994*