(EC526) FPGA & CPLD ARCHITECTURES AND APPLICATIONS

Objective of the Course : *Student will acquire the knowledge of building blocks of DSP processors, Architectural, programming issues of 54XX series DSP processor and its interfacing*

UNIT - I

Programmable logic : ROM, PLA, PAL, PLD, PGA – Features, programming and applications using complex programmable logic devices Altera series – Max 5000/7000 series and Altera FLEX logic – 10000 series CPLD, AMD's – CPLD (Mach 1 to 5); Cypres FLASH 370 Device Technology, Lattice pLSI's Architectures – 3000 Series – Speed Performance and in system programmability.

UNIT - II

FPGAs: Field Programmable Gate Arrays – Logic blocks, routing architecture, Design flow, Technology Mapping jfor FPGAs, Case studies – Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T –ORCA's (Optimized Reconfigurable Cell Array): ACTEL's – ACT-1,2,3 and their speed performance.

UNIT - III

Finite State Machines (FSM): Top Down Design – State Transition Table, state assignments for FPGAs. Problem of initial state assignment for one hot encoding. Derivations of state machine charges. Realization of state machine charts with a PAL. Alternative realization for state machine chart suing microprogramming. Linked state machines. One – Hot state machine, Petrinetes for state machines – basic concepts, properties. Extended 4petrinetes for parallel controllers. Finite State Machine – Case Study, Meta Stability, Synchronization.

UNIT - IV

FSM Architectures and Systems Level Design: Architectures centered around non-registered PLDs. State machine designs centered around shift registers. One – Hot design method. Use of ASMs in One – Hot design. K Application of One – Hot method. System level design – controller, data path and functional partition.

UNIT - V

Digital Front End Digital Design Tools for FPGAs & ASICs: Using Mentor Graphics EDA Tool ("FPGA Advantage") – Design Flow Using FPGAs – Guidelines and Case Studies of paraller adder cell, paraller adder sequential circuits, counters, multiplexers, parallel controllers

REFERENCE BOOKS:

1. P.K.Chan & S. Mourad, "Digital Design Using Field Programmable Gate Array", jPrentice Hall (Pte), 1994.
2. S.Trimberger, Edr., "Field Programmable Gate Array Technology", Kluwer Academic Publicatgions, 1994.
3. J. Old Field, R.Dorf, "Field Programmable Gate Arrays", John Wiley & Sons, Newyork, 1995.
4. S.Brown, R.Francis, J.Rose, Z.Vransic, "Field Programmable GateArray", Kluwer Pubin, 1992.