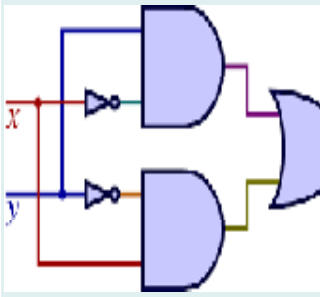
16CS203 DIGITAL LOGIC DESIGN



Hours Per Week :

L	T	P	C
3	1	-	4

Total Hours :

L	T	P
45	15	-

CS	WA/RS	SSH	SA	S	BS
7	5	40	8	2	2

Course Description and Objectives:

This course introduces the topics such as number systems, analysis and design of combinational and sequential circuits, digital circuit design optimization methods using multiplexers, decoders, registers, counters and programmable logic arrays. The objective of this course is to offer the knowledge and skill of conversions between different number systems, design of logical gates, minimization of switching functions, effective memory utilization and design of synchronous and asynchronous counters.

Course Outcomes:

The student will be able to:

- determine philosophy of number systems and codes.
- minimize switching functions using Boolean algebra, Karnaugh maps and tabular method.
- design combinational and sequential logic circuits using conventional gates.
- gain knowledge of the ROM, RAM, PROM, PLD etc.

SKILLS :

- ü *Perform number conversion.*
- ✓ *Synthesize boolean algebra.*
- ✓ *Construct combinational circuits like, decoders, encoders, multiplexers etc.*
- ✓ *Analyze counters, shift registers etc.*
- ✓ *Construction of PLA and PLD.*

ACTIVITIES:

- *Design of logical circuits using universal gates and basic gates.*
- *Reduction of Boolean function using K-maps.*
- *Construction of one stage ALU circuit.*
- *Design of the n-bit decoder and encoder.*
- *Design of combinational circuits using different types of flip-flops.*
- *Design of PLA for the given Boolean expression.*
- *Design of PLD for the given Bolean expression.*
- *Design of different types of counters.*

UNIT - 1 **L-09,T-03**

NUMBER SYSTEMS AND BOOLEAN ALGEBRA: Number system **-** Binary numbers, Number base conversions, Octal and hexadecimal numbers, Complements of numbers, Signed binary numbers, Binary codes, Binary logic. Boolean Algebra **-** Basic definitions, Basic theorems and properties of Boolean algebra.

UNIT - 2 **L-09,T-03**

LOGIC GATES AND GATE-LEVEL MINIMIZATION: Boolean functions, Canonical and standard forms, Digital logic gates, The map method, Four - variable k-map, Product-of-sums simplification, Don't-care conditions, NAND and NOR implementation, Other two-level implementations, Exclusive-or function.

UNIT -3 **L-09,T-03**

COMBINATIONAL LOGIC: Combinational circuits, Analysis and design procedure, Binary adder–subtractor, Decimal adder, Binary multiplier, Magnitude comparator, Decoders, Encoders, Multiplexers, De-mutliplexers.

UNIT - 4 **L-09,T-03**

SEQUENTIAL LOGIC: Sequential circuits, Storage Elements-Latches, Flip-flops, Analysis of clocked sequential circuits, Design procedure, Registers, Counters.

UNIT - 5 **L-09,T-03**

PROGRAMMABLE LOGIC DEVICES: Programmable logic, PLDs, ROM, Types of ROM, Combinational Programmable Devices, Programmable Logic Array, Programmable Read Only Memory.

TEXT BOOK:

1. M Morris Mano and Michael D. Ciletti, " Digital Design", 5th edition, Pearson Education, Inc, 2013.

REFERENCE BOOKS:

1. H Taub and D Schilling, "Digital Integrated Electronics", 2nd edition, TataMc Graw-Hill, 2004.
2. Z. Kohavi, "Switching and Finite Automata Theory", 2nd edition, Tata McGraw-Hill,2008.