SOME NEW OPERATIONAL TRANSRESISTANCE AMPLIFIER BASED SINUSOIDAL/SQUARE WAVEFORM GENERATORS

A THESIS

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OCTOBER 2016

Dedicated

to

My family

DECLARATION

I hereby declare that the work reported in the Ph.D. thesis entitled **"SOME NEW OPERATIONAL TRANSRESISTANCE AMPLIFIER BASED SINUSOIDAL/SQUARE WAVEFORM GENERATORS"** submitted at **Vignan's Foundation for Science, Technology and Research University,** Vadlamudi, India, is an authentic record of my work carried out under the supervision of **Prof. Avireni Srinivasulu**. I have not submitted this work elsewhere for any other degree or diploma.

(CHANDRA SHEKAR PITTALA)

THESIS CERTIFICATE

This is to certify that the thesis entitled **SOME NEW OPERATIONAL TRANSRESISTANCE AMPLIFIER BASED SINUSOIDAL/SQUARE WAVEFORM GENERATORS** submitted by **CHANDRA SHAKER PITTALA** to the Vignan's University, Vadlamudi, Guntur, for the award of the degree of **Doctor of Philosophy** is a bonafide record of the research work done by him under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

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ABSTRACT

SOME NEW OPERATIONAL TRANS-RESISTANCE AMPLIFIER BASED SINUSOIDAL/SQUARE WAVEFORM GENERATORS

KEYWORDS: Analogue signal processing blocks, Duty cycles, Operational transresistance amplifier, Oscillators, Square waveform generators, Waveform generators.

Waveform generators have wide range of applications in numerous electronic devices, including electronic instruments, measurement systems, telecommunications, power conversion control circuits and signal processing applications. Several waveform generator circuits have existed in the literature based on operational amplifier (op-amp) as a main active element. However, these circuits are not able to operate at high frequency due to fixed gain bandwidth product and less slew rate.

To conquer the above disadvantages several circuits have been presented in the literature based on current-mode devices. When wide bandwidth, low power consumption and low voltage operation are needed simultaneously, current mode devices are preferred rather than voltage mode devices. Current mode circuits feature the advantage of high bandwidth, better linearity, larger dynamic range and non-interference between the gain and bandwidth.

In recent past, an active current mode device operational transresistance amplifier (OTRA) has made considerable attention of the analog IC designers. OTRA is a three terminal active device. Several implementations have emerged using OTRA such as Voltage Gain Amplifiers (VGAs), filters, Proportional Integral and Derivative (PID) controllers, analogue multiplier, immitance simulators, oscillators and waveform generators.

Sinusoidal waveform generators with independent control of condition of oscillation and frequency of oscillation play an important role in communications and signal processing application. It has also been seen that the OTRA is very useful as an analogue building block and receiving regular attention in waveform generators, oscillators, and design of amplifiers and filters. The OTRA provides a constant bandwidth virtually independent of the gain. Characterized by low input and output

impedances, it leads to circuits that are insensitive to stray capacitances, providing current processing at the input terminal which are virtually grounded.

In this thesis, a generalized configuration with a grounded passive component is proposed to realize few sinusoidal oscillator circuits. A minimum component oscillator circuit, eight grounded passive component sinusoidal oscillator circuits and two sinusoidal oscillator circuits with grounded resistance and capacitance are realized from the generalized configuration.

Quadrature oscillator is an important building block for many electronics and communication applications. Part of this thesis discusses two quadrature sinusoidal oscillator circuits with independent control of condition of oscillation and frequency of oscillation. In addition, two square waveform generators and their advantages with respect to the existing square waveform generators in the literature are presented in detail.

The operation principles and non-idealities of all the proposed circuits are described in detail. All the proposed circuits are designed and developed using Cadence 0.18 μm CMOS model parameters. The proposed OTRA based circuits can be operated at ± 1.8 V supply voltages. The performances of the circuits are explored through Spectre simulation model parameters. The proposed circuits are also designed and checked for waveform generation on a laboratory bread board using IC AD 844 AN.

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ABBREVIATIONS

CC	Current Conveyor
CC-CDBA	Current Controlled Current Differencing Buffered Amplifier
CCCDTA	Current Controlled Current Differencing Transconductance Amplifier
CCII	Second-Generation Current Conveyor
CDBA	Current Differencing Buffered Amplifier
CDTA	Current Differencing Transconductance Amplifier
CFOA	Current Feed-Back Operational Amplifier
CMOS	Complementary Metal Oxide Semiconductor
DCCCS	Differential Current Controlled Current Source
DCCII	Second Generation Differential Current Conveyor
FTFN	Four Terminal Floating Nuller
IC	Integrated Circuit
JFET	Junction Field Effect Transistor
KCL	Kirchhoff's Current Law
MDCC	Modified Differential Current Conveyor
MOS-C	MOSFET and Capacitors
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
OTA	Operational Transconductance Amplifier
OTRA	Operational Transresistance Amplifier
PID	Proportional Integral and Derivative
RF	Radio Frequency
VCVS	Voltage Controlled Voltage Source
VDTA	Voltage Differencing Transconductance Amplifier
VDBA	Voltage Differencing Buffered Amplifier
VGA	Voltage Gain Amplifiers
VLSI	Very Large Scale Integration

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION TO CURRENT-MODE CIRCUITS

Sinusoidal/square waveform generators are the basic building cells in many electronic circuit systems. For example, in instrumentation, measurement systems, communication systems, power conversion control circuits and signal processing application [1]. The sinusoidal and square waveform generators along with other circuits are often employed to produce various standard signals, such as triangular wave, pulse wave, etc. Since the introduction of integrated circuits, the operational amplifier (op-amp) has been serving as the basic building block in many electronics circuit designs. Since then, new integrated analogue circuit applications have emerged and the performance requirements for analogue circuits have changed. A typical voltage-mode waveform generator can be implemented by using an op-amp with a few passive components. Verities of waveform generators using voltage mode op-amp are available in the literature [2, 3]. These voltage-mode (op-amp) circuits yield some drawbacks such as complex internal circuitries, lower slew rate, constant gain bandwidth product and more passive components are however required to generate the waveforms. The finite gain bandwidth product of an op-amp affects the performance of the waveform generator. Furthermore, the limited slew rate of the op-amp affects the large signal and high frequency operations [4-6]. Analogue circuit design has historically been dominated by voltage-mode signal processing. In voltage-mode, current signals are transferred into a voltage domain before any analogue signal processing. This makes an integrated circuit (IC) unsuitable for low voltage application. When low voltage, low power consumption and wide bandwidth are required simultaneously, the voltage-mode devices easily become too complex and failed to achieve the required characteristics [7]. The performance of a circuit in analogue circuits is determined in terms of voltage levels at the different nodes in the circuit including input and output nodes are known as voltage mode circuits. Large output voltage swing while minimizing the total power consumption is required to provide in voltage mode circuits. This causes high impedance node architecture in the voltage mode circuits. In voltage mode circuits with large voltage swing, the parasitic

capacitances presented in the circuits need to be charged and discharged, this leads to decrease of the speed and slew rate in the voltage mode circuits.

Apart from the op-amps or voltage-mode approaches, another circuit design concept, current-mode technique was introduced [4-7]. The current mode circuits are low impedance circuits. The performance of the current mode circuits in terms of speed and slew rate is very high compared to the voltage mode circuits. By using the current signals instead of voltage signals, the current mode circuits are able to operate with low supply voltages. The addition opeartion in current mode circuit is much easier than the voltage mode circuits. By using KCL (Kirchhoff's Current Law), the addition and subtraction is possible by joining the terminals at a node in the current mode circuit. This eliminates the passive components, reduces the power consumption and chip area compared to the voltage mode. In addition to the above stated advantages, the dynamic range of the current mode circuits is larger than that of the voltage mode circuits. The first current-mode based active device named current conveyor (CC) was introduced in 1968 [6]. Since then, many new active current-mode devices have been reported in the literature [8-17]. Second and third generation current conveyors were introduced in 1970 and 1995 [6]. The terminal relations for the first, second and third generation current conveyors are different. Based on the output terminal current direction, the current conveyors are further classified as CCII+ and CCII-. The Operational Transconductance Amplifier (OTA) is used to drive the capacitive loads [8]. Many applications are available in the literature using Current Feed-back Operational Amplifier (CFOA) [9]. CFOA has the similar terminal relation with respect to the CCII. Few current mode devices are listed below.

i) Four Terminal Floating Nuller (FTFN)
ii) Current Differencing Buffered Amplifier (CDBA)
iii) Current Controlled CDBA (CC-CDBA)
iv) Current Differencing Transconductance Amplifier (CDTA)
v) Current Controlled CDTA (CCCDTA)
vi) Voltage Differencing Transconductance Amplifier (VDTA)
vii) Voltage Differencing Buffered Amplifier (VDBA)

In previous researches, some waveform generators were presented based on current-mode devices [18-30]. These current-mode waveform generators have attracted much attention of the analogue integrated circuit designers due to the

advantages over voltage mode waveform generators such as; the oscillation frequency can be adjusted more accurately, the oscillation frequency is less sensitive to the bandwidth variation of the active devices and because of the large slew rate, the current-mode oscillator can achieve higher frequencies at larger amplitude levels.

1.2 MOTIVATION OF THE WORK

The modern integrated circuit technologies are normally developed to be driven by the needs of digital CMOS circuit design. As the size of integrated devices decreases, so maximum voltage ratings are also rapidly reduces. Although decreased supply voltages do not restrict the design of digital circuits, it is harder to design high performance analogue integrated circuits using new processes. In digital integration technologies, there are fewer integrated devices available for the circuit design. In the worst case situation, this means that only transistors are available for analogue circuit design. There may occasionally be capacitances and resistors, but their values may be small and there are significant parasitic components present. Thus, if we want to utilize the fastest integration technologies available, which are normally restricted to the active components in the design of integrated analogue circuits. Since the introduction of integrated circuits, the operational amplifier has served as the basic building block in analogue circuit design. When signals are widely distributed as voltages, the parasitic capacitances are charged and discharged with the full voltage swing, which limits the speed and increases the power consumption of voltage-mode circuits.

One procedure for finding alternative, preferably simpler, current-mode approach is preferred rather than the traditional voltage-mode structures for signal processing [4-7]. Current-mode circuits cannot avoid nodes with high voltage swing either, but these are usually local nodes with less parasitic capacitances. Therefore, it is possible to reach higher speed and lower dynamic power consumption with current-mode circuit techniques. Since the concept of the current conveyor was brought into being, there are many current-mode analogue building blocks developed and the related applications have been reported in the literature [8-30].

In the past few years, an active device called Operational Transresistance Amplifier (OTRA) is reported and applied [31-38]. Several OTRA-based implementations have emerged. OTRA, being a current processing analogue building

block, inherits all the advantages of the current mode technique and therefore is ideally suited for high frequency applications [39-43]. It is also free from parasitic input capacitances and resistances as its input terminals are virtually grounded and hence, non-ideality problem is less in circuits implemented with OTRA. Low input, output impedances and device gain which is bandwidth independent are the main advantageous properties of the OTRA. The OTRA has also been using as one of the basic building blocks in the field of analogue signal processing [44-60]. OTRA is designed for low voltage operation, low power consumption, wide bandwidth, high speed, greater linearity and simpler circuit complexity. Several circuits for different applications have been reported in the literature [61-88] based on OTRA as a main active element, such as instrumentation amplifiers, MOSFET-C differentiator, integrators, continuous-time filters, immitance simulators, waveform generators, bistable multivibrators and oscillators.

1.3 OBJECTIVES

In the last decade, few number of current-mode sinusoidal/square waveform generators were introduced in the area of analogue signal processing. However, the researchers still aim to design and develop new waveform generator circuits to improve the characteristics of the existing circuits to achieve better features than their counterparts. These better features can be described as less number of passive components, and less number of active components, high frequency performance/inherent signal bandwidths, greater linearity, lower power consumption, lower supply voltages and simplicity in circuit designing. Sinusoidal/square waveform generators are widely used in analogue signal processing. Few sinusoidal/square waveform circuit realizations using different active building blocks have been reported in the literature. These circuit realizations have some drawbacks such as more active/passive components.

Therefore, the main aim of this thesis is to design, develop and testing of new sinusoidal/square waveform generators. The first intention is to design a generalized configuration for the sinusoidal oscillator with one active component, minimum number of passive components and a grounded resistor/capacitor. By using this generalized configuration a few number of oscillator circuits can be realized. The oscillator circuits, which are realized from the generalized configuration, are

controlled by the single grounded resistance/capacitance. Quadrature oscillator is an important building block in many communication, control systems, instrumentation and measurement systems. Therefore, part of this work is attempted on this issue.

The square-wave generator is widely operated in many electronic fields such as digital, instrumentation and communication systems. Conventional square waveform generator circuits pose some drawbacks such as complex internal circuitries, lower slew rate, constant gain bandwidth product, more passive components and non-linear variation of the time period with respect to the passive components. Hence, the intension is to design a square-wave generator with minimum number of passive components, one active component and improved linearity with respect to the passive components connected to the circuit.

In the first step the theoretical analysis is done. To verify the behaviour of the proposed circuits, OTRA is implemented with CMOS transistors and checked for waveform generation. The feasibility of the proposed circuits is also confirmed by the experimental measurements.

1.4 ORGANIZATION OF THESIS

Chapter (2) deals with an introductory overview of the operational transresistance amplifier (OTRA) and its CMOS implementation. Three CMOS OTRA implementations are discussed in this chapter. These CMOS OTRA implementations are already reported in [32-35]. Two of these CMOS OTRA implementations are based on the modified differential current conveyor (MDCC) and a common source amplifier. The OTRA implemented with differential current controlled current source (DCCCS) followed by a buffer [35] is discussed. The operation of these three OTRAs is studied and simulated using Cadence gpdk 180 nm CMOS model parameters.

Chapter (3) provides the background review of the existed waveform generators by using OTRA. Two square waveform generators, one square/triangle waveform generator and some sinusoidal oscillator circuits existed in the literature [46-58] are discussed in this chapter. These circuits are designed and simulated using Cadence Spectre simulation model parameters. The advantages of these circuits are quoted and their drawbacks have been detected during the implementation and simulation is given in this chapter.

Chapter (4) introduces some new waveform generator circuits. In this chapter, a generalized configuration for sinusoidal oscillator circuits, two quadrature sinusoidal oscillators and two square waveform generator using OTRA are proposed. The generalized configuration proposed in this chapter is used to produce few sinusoidal oscillator circuits. The operations of the proposed circuits to produce oscillations are discussed in detail. The quadrature sinusoidal oscillators and square waveform generators operations are discussed in this chapter.

Chapter (5) describes the mathematical analysis of the proposed circuits in chapter 4. The basic network laws and ideal terminal characteristics of OTRA are applied to the proposed circuits to derive the oscillation frequency and condition of oscillations for the oscillator circuits realized from the generalized configuration. Similarly, the same procedure is applied to derive the mathematical equations for the quadrature sinusoidal oscillators and square waveform generators.

Chapter (6) deals with the non-ideal analysis of the proposed circuits. The transresistance gain of the OTRA is infinite in an ideal case. But, practically, the OTRA transresistance gain is finite and its effect should be considered. In this chapter, all the proposed circuits in chapter (4) are reanalyzed based on non-ideal characteristics of OTRA.

Chapter (7) deals with the simulation results of the proposed circuits in chapter (4). All the proposed circuits are checked for waveform generation by connecting with passive components. The passive component values are calculated from the mathematical equations derived in chapter (5). All the proposed circuits are simulated using Cadence Spectre simulation model parameters. Further the simulation results are presented in this chapter to validate the mathematical analysis carried out in chapter (5).

Chapter (8) presents hardware implementation of the proposed circuits on a laboratory bread board. The OTRA prototype circuit is implemented by using two AD844 AN ICs and external passive components are connected to test the waveform generation of the proposed circuits. The proposed circuits are tuned for different passive component values. Hardware results are given in this chapter to validate the simulation and theoretical analysis.

Chapter (9) presents the advantages of the proposed circuits compared to the existing circuits in the literature based on OTRA. In the end, conclusions and future scope are given in this chapter.

CHAPTER 2

OPERATIONAL TRANSRESISTANCE AMPLIFIER (OTRA)

2.1 INTRODUCTION

As signal processing extends to higher frequencies, circuit designers are detected, that the traditional design methods based on voltage op-amps are no longer adequate. It is well known that the traditional operational amplifiers have a bandwidth which is dependent on the closed loop voltage gain [1-7]. The attempt to overcome this problem has led to the interest in circuits which operate in current-mode. These circuits employ current processing techniques to improve dynamic speed capability, providing a constant bandwidth virtually independent of the gain. In the last decade, a new current mode device called an operational transresistance amplifier attracted considerable attention of the analogue IC designers. The operational transresistance amplifier is a high gain current input and voltage output analogue building block [31-44]. The circuit symbol of the OTRA is shown in Fig. 2.1. The input and output terminal relations of an OTRA can be characterized by matrix given below Fig. 2.1. For ideal operation, the transresistance gain R_m approaches infinity forcing the input currents to be equal. Low input and output impedances, a bandwidth independent of the device gain can be considered as the main advantage of the OTRA. Current differencing amplifier and Norton amplifier are the commercially available names of OTRA. These commercial realizations allow input current to flow only in one direction and do not have internal ground at the input terminals. The former disadvantage, limited the functionality of the OTRA, whereas, the latter forced to use external DC bias current leading complex and unattractive designs.

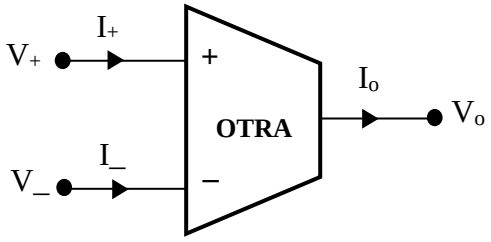


Fig. 2.1 OTRA circuit symbol

$$\begin{bmatrix} V_+ \\ V_- \\ V_0 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_+ \\ I_- \\ I_0 \end{bmatrix} \quad (2.1)$$

$$V_+ = V_- = 0 \quad (2.2)$$

$$V_o = I_+ R_m - I_- R_m \quad (2.3)$$

In order to overcome these disadvantages of the OTRA, some topologies are proposed in the literature, second generation current conveyor based OTRA implementation is proposed in [32, 35] and [36]. A new norton amplifier based OTRA on current follower configuration with class-AB output stage for low power realization is proposed in [37] and also shows a fully differential implementation to reduce the accurate matching required for current matching. A new CMOS fully differential OTRA design for the low voltage with low power supplies in the submicron technology is reported in [41].

2.2 CMOS OPERATIONAL TRANSRESISTANCE AMPLIFIER (OTRA)

2.2.1 SALAMA OTRA

In OTRA both the input and output terminals are characterized by low impedance, thereby eliminating response limitations incurred by capacitive time constants. The input terminals are virtually grounded leading to circuits that are insensitive to stray capacitance. Ideally, the transresistance gain, R_m, approaches infinity and forces the two input currents I_+ and I_- to be equal. Practically, the transresistance gain is finite and its effect should be considered along with finite input resistance, output resistance and the frequency limitations associated with the OTRA. Fig. 2.2 shows a simple, non-ideal model of the OTRA with a finite input and output resistance. The input terminals are not virtually grounded, but at a finite voltage determined by the finite input resistance. Also the output voltage is determined by the finite output resistance and the input offset difference current.

Salama *et al.*, proposed a CMOS OTRA circuit based on the modified differential current conveyor circuit (MDCC) and a common source amplifier [32]. The common source amplifier provides the high gain stage and MDCC provides the current

differencing operation. The CMOS implementing of salama OTRA is shown in Fig. 2.3.

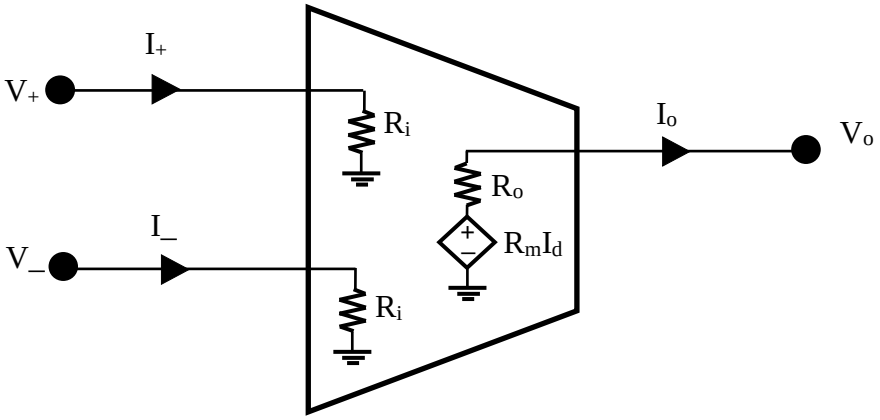


Fig. 2.2 Non-ideal model of OTRA

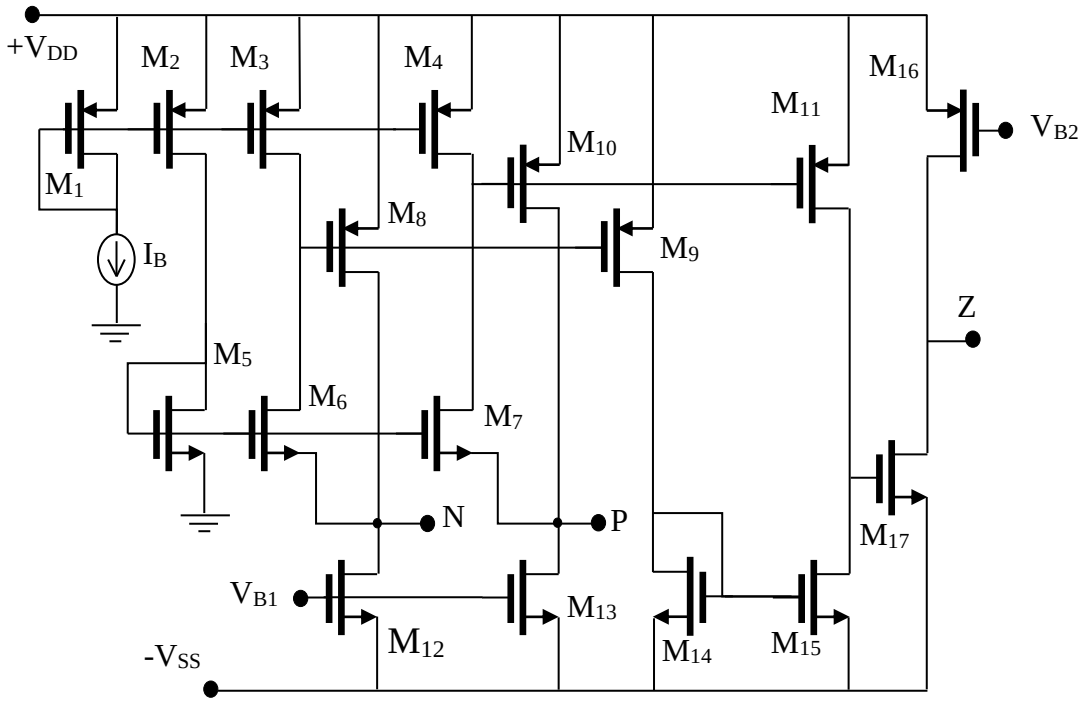


Fig. 2.3 CMOS implementation of the Salama OTRA

Assuming all the transistors are operating in the saturation region, the circuit operation can be explained as follows. The current mirror formed by (M_1-M_4) forces equal current (I_B) in the transistors M_5, M_6 and M_7. This operation derives the gate to source voltages of M_5, M_6 and M_7 to be equal and, consequently, forces the two input terminals to be virtually grounded. The current mirrors formed by the transistor pairs M_3 and M_4; M_8 and M_9; M_{10} and M_{11}; M_{14} and M_{15} provide the current differencing

operation, whereas, the common source amplifier formed by M_{17} achieves the high gain stage. The current biasing I_B, is connected to the transistors M_1 with common gate and thus biases the transistors M_1 to M_4. Transistors M_3, M_6, M_8, M_9 and M_4, M_7, M_{10}, M_{11} form two loops which transmit the current I_P and I_N respectively. Hence the output voltage is produced with currents of M_9 and M_{11}, which biases the output stage transistors in the OTRA design.

2.2.2 SIMULATION RESULTS

The performance of the Salama OTRA is simulated using Cadence Spectre simulation models and its basic functionality with a central value of specifications at a specific biasing and sizing conditions of the circuit is estimated.

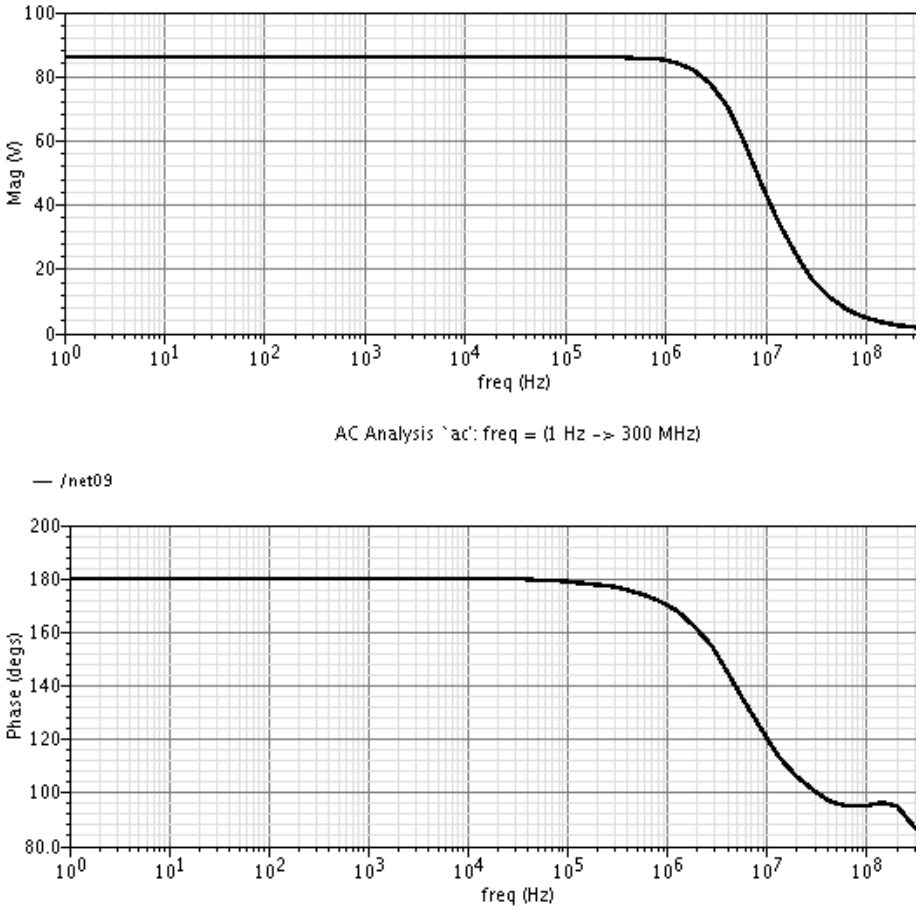


Fig. 2.4 Frequency response of the Salama OTRA

The biasing current I_B = 5 µA, biasing voltages V_{B1} = -1 V and V_{B2} = 1.8 V are used for the simulation of Salama OTRA. Fig. 2.4 shows the magnitude and phase response simulation results of the Salma OTRA. From this AC characteristic, the open loop transresistance gain of the OTRA is 80.1 dBΩ and the transresistance gain bandwidth is 11.3 MHz. Fig. 2.5 shows the output voltage of the OTRA for different

values of inverting input and non-inverting input currents. From this plot, the input current differential range is from -30 µA to +30 µA. The input resistance plot for the Salama OTRA is shown in Fig. 2.6 and the output resistance plot is shown in Fig. 2.7. The Salama OTRA is simulated with a supply voltage of ± 1. 8 V.

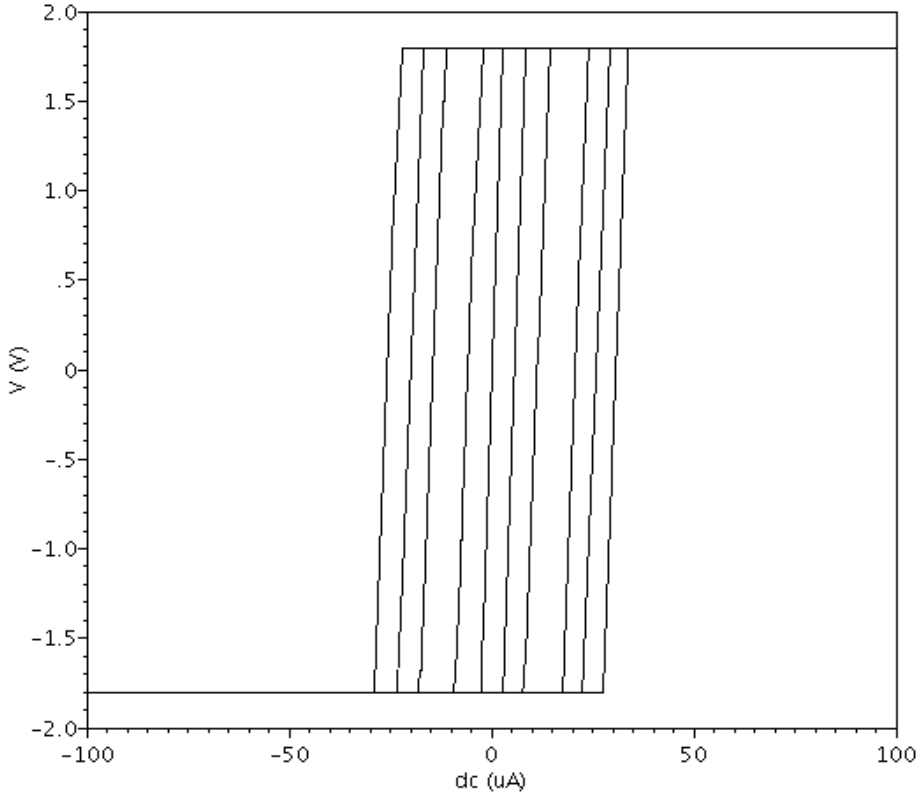


Fig. 2.5 Output voltage at terminal Z in Fig. 2.3

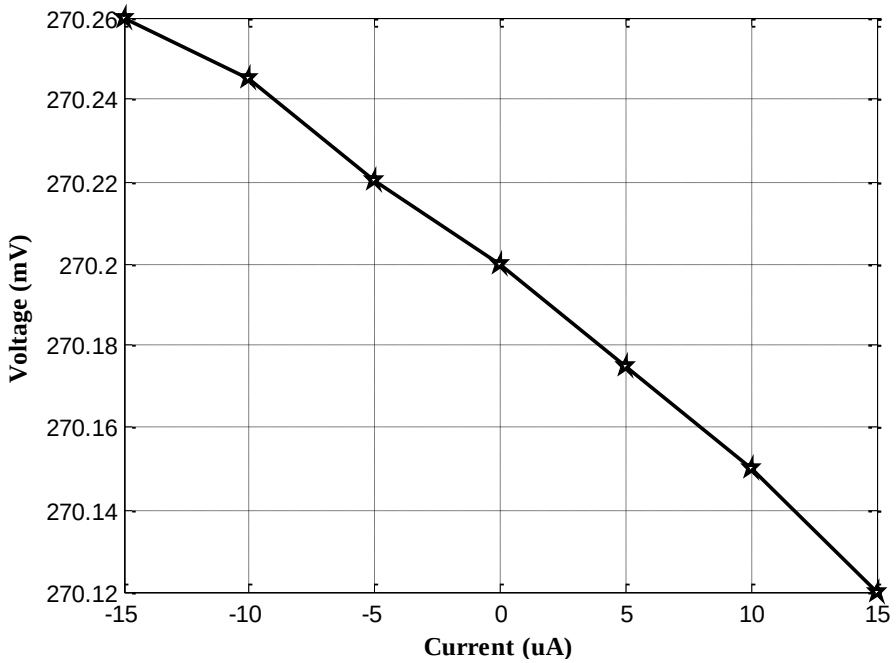


Fig. 2.6 Input resistance plot for the circuit in Fig. 2.3

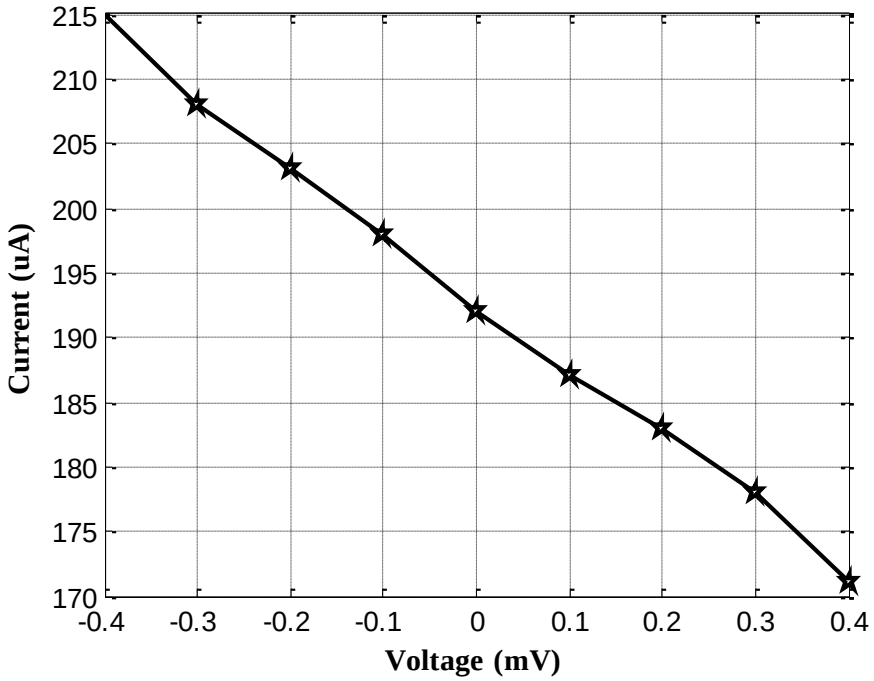


Fig. 2.7 Output resistance plot for the circuit in Fig. 2.3

2.2.3 OTRA USING A CURRENT DIFFERENCING BUFFERED AMPLIFIER

Ali Toker *et al.*, proposed a new CMOS implementation for current differencing buffered amplifier (CDBA) in [33]. The CDBA can easily be implemented by CMOS transistors by using the configuration shown in Fig. 2.8. This CDBA CMOS implementation can also be used as OTRA and current feedback operational amplifier (CFOA). This CMOS implementation consists of a differential current controlled current source (DCCCS) followed by a voltage buffer. Assuming all the transistors are in the saturation region, the circuit operation is explained as follows. The current mirrors formed by the transistors M_1, M_3 and M_5 forces equal currents in the transistors M_9 and M_{10}. The current mirrors M_2, M_4 and M_6 forces equal current in the transistors M_7 and M_8. M_1 and M_2 transistors sources are connected to ground. This operation makes the gate to source voltages of the transistors M_1-M_6 to be equal and consequently, forces the two input terminals to be virtually grounded. The current mirror transistors from M_1 to M_{10} and transistors M_{11} and M_{12} provides current differencing operation, whereas, the rest of the circuit provides a high gain stage. The bias currents I_0 are given to biases the transistors M_1-M_6. By removing the output terminal W in the CMOS implementation shown in Fig. 2.8, it will be converted as OTRA. The transistor M_5 and M_6 can be removed to form a CFOA.

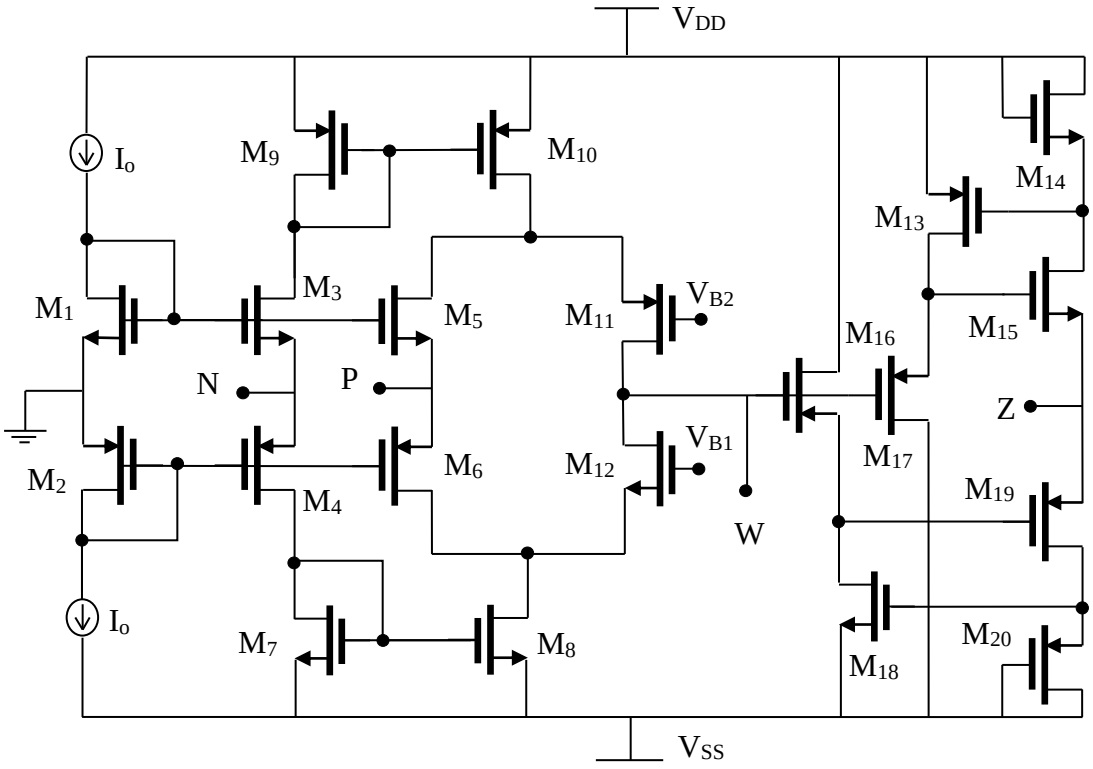


Fig. 2.8 Device level implementation of OTRA

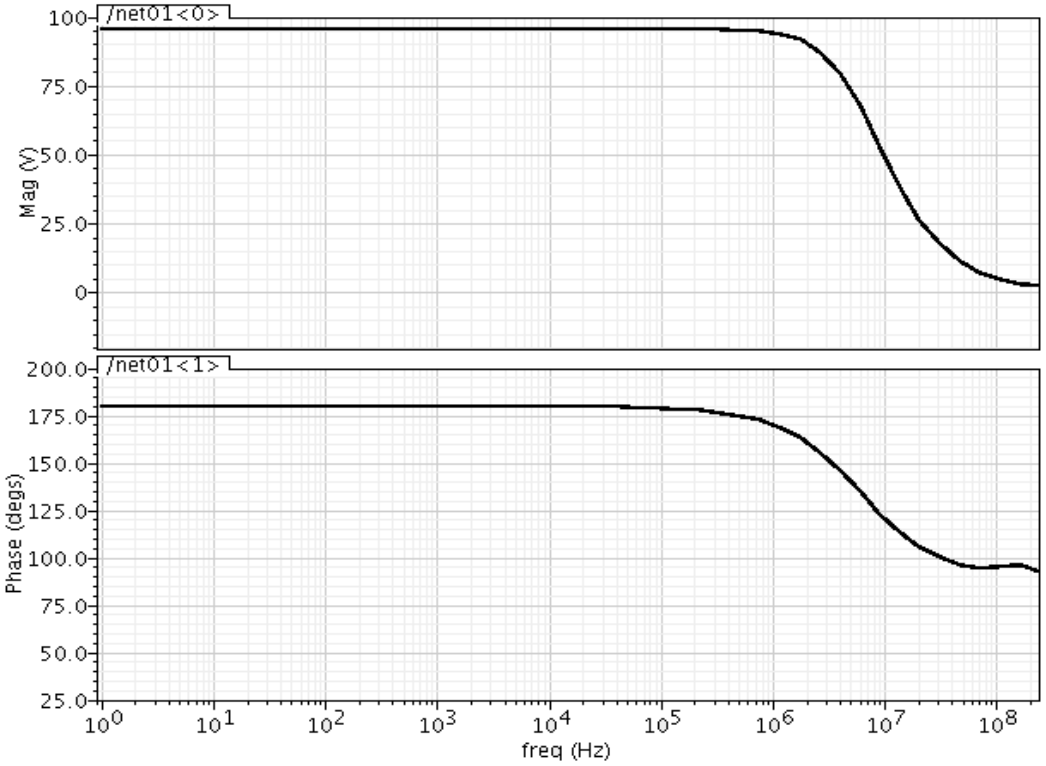


Fig. 2.9 Frequency response of the CMOS circuit shown in Fig. 2.8

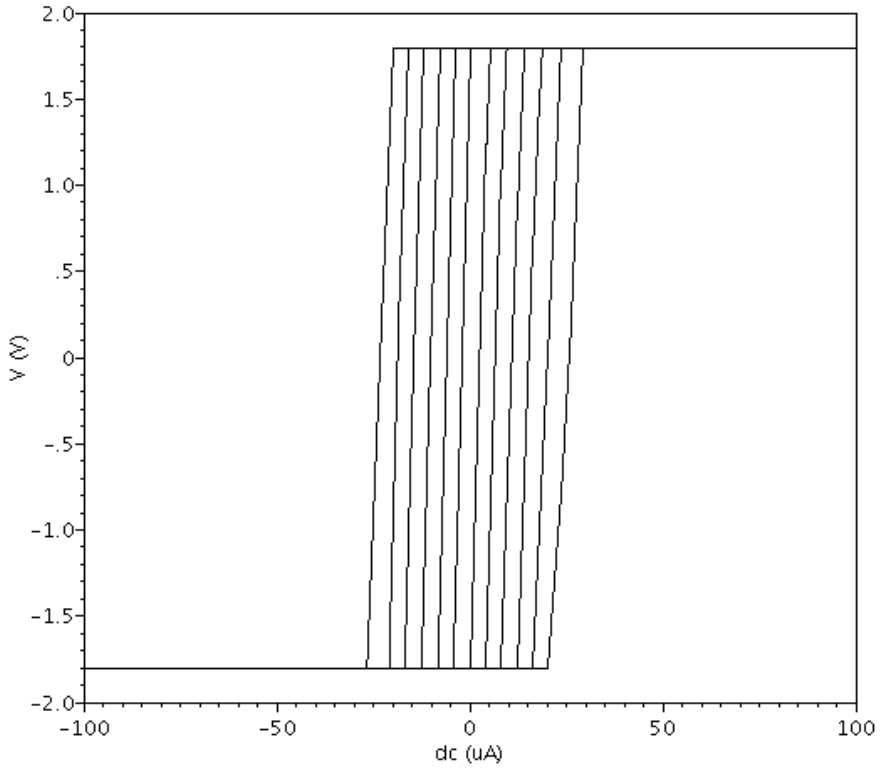


Fig. 2.10 Output voltage at terminal Z in Fig. 2.8

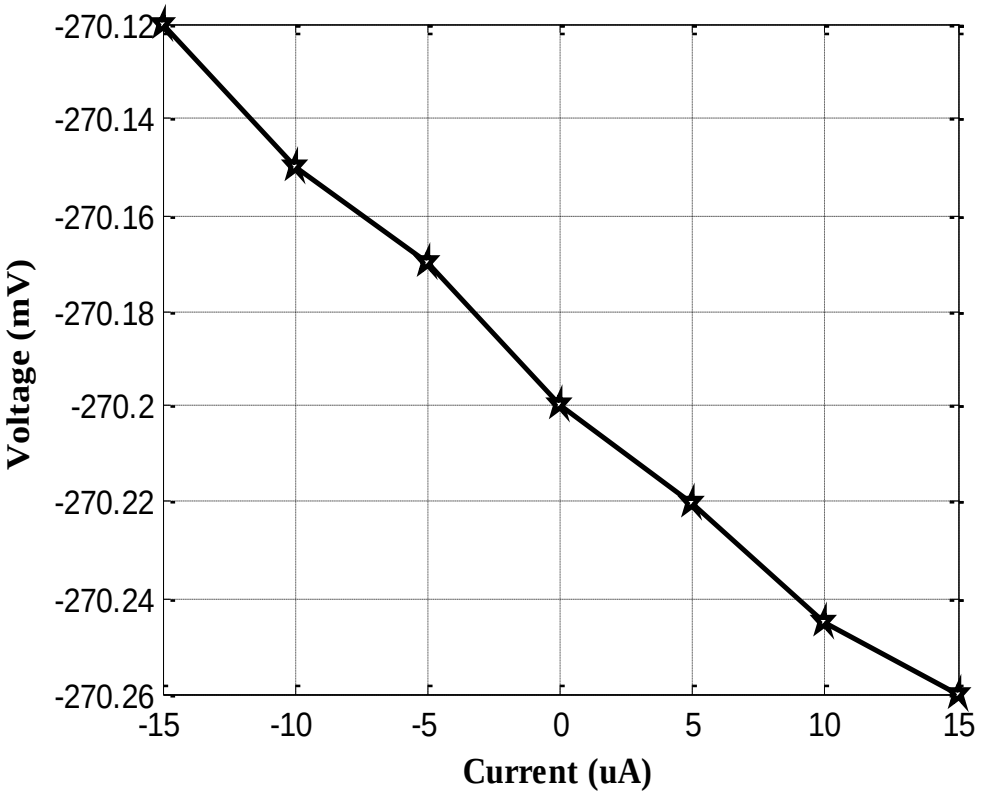


Fig. 2.11 Input resistance plot for the circuit shown in Fig. 2.8

2.2.4 SIMULATION RESULTS

The functionality of the CMOS OTRA shown in Fig. 2.8 is simulated by using Cadence Spectre simulation models. The biasing current I_o = 20 µA, biasing voltage V_{g1} = 0.8 V and V_{g2} = -0.8 V with a supply voltage of ± 1.8 V is applied to the CMOS circuit shown in Fig. 2.8. The magnitude and phase response simulation results of the OTRA depicted in Fig. 2.8 is shown in Fig. 2.9. From this AC characteristic, the open loop transresistance gain of the OTRA is 93.31 dBΩ and the transresistance gain bandwidth is 5.3 MHz. The output voltage of the OTRA for different values of inverting input and non-inverting input currents is shown in Fig. 2.10. The input and output resistance plots are sown in Fig. 2.11 and 2.12.

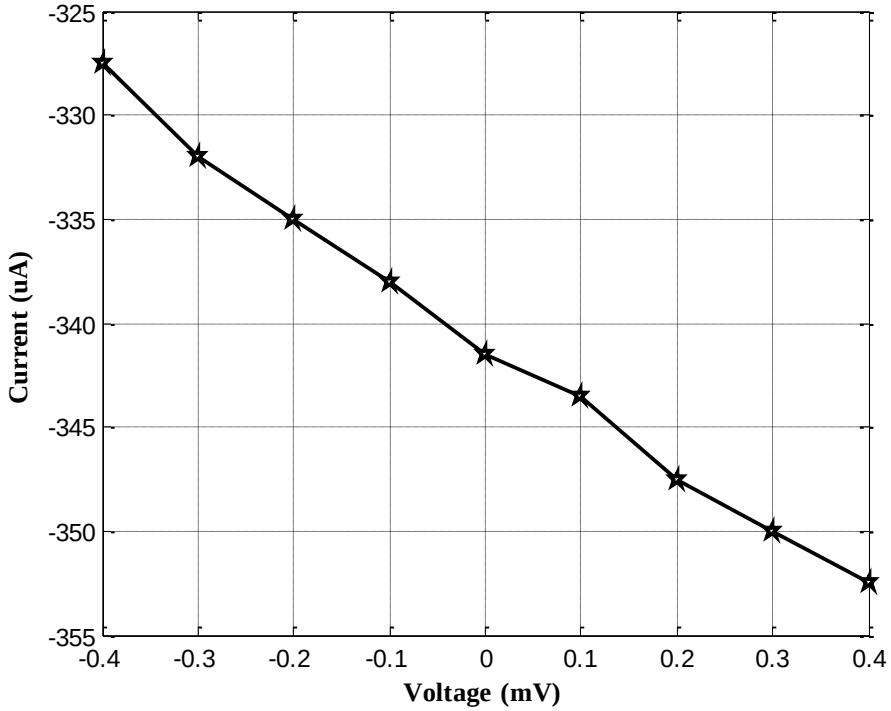


Fig. 2.12 Output resistance plot for the circuit shown in Fig. 2.8

2.3 OTRA IMPLEMENTATION USING IC AD 844

The operational transresistance amplifier can also be implemented using the commercially available IC called a current feedback operational amplifier (CFOA) AD 844 AN [46-49]. The CFOA is a three terminal active device. The circuit symbol of the CFOA is shown in Fig. 2.13. The OTRA implementation using the IC AD 844 AN is shown in Fig. 2.14. Two AD 844 AN ICs and a resistor are used to construct the OTRA. The non-inverting terminals of the AD 844 ANs have been grounded, to

simulate the virtual ground, for the terminals of the OTRA. The following equations can be obtained from the Fig. 2.14.

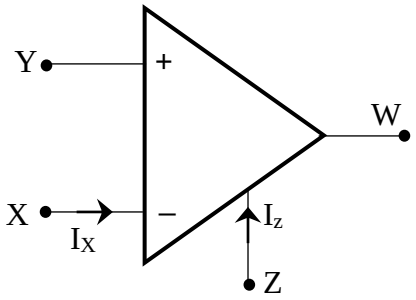


Fig. 2.13 CFOA (AD 844) circuit symbol

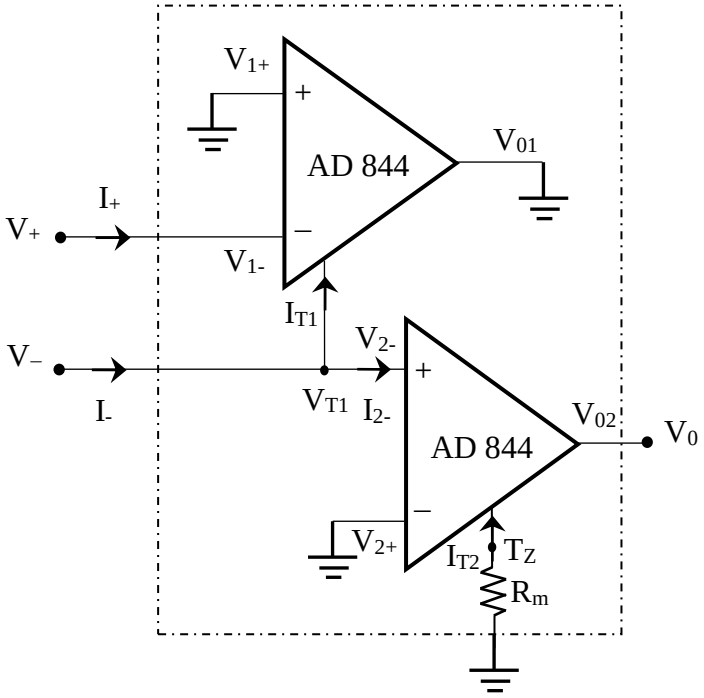


Fig. 2.14 Implementation of OTRA using AD 844 ICs

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \\ V_W \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \\ I_W \end{bmatrix} \tag{2.4}$$

$$V_+ = V_{1-} = V_{1+} = 0 \tag{2.5}$$

$$V_{-} = V_{2-} = V_{2+} = 0 \tag{2.6}$$

$$V_{01} = V_{T1} = V_{2-} = V_{2+} = 0 \tag{2.7}$$

$$I_{T1} = I_{1-} = I_{+} \tag{2.8}$$

$$I_{T2} = I_{2-} = I_{-} - I_{T1} = I_{-} - I_{+} \tag{2.9}$$

$$V_0 = V_{T2} = -R_m \times I_{T2} = R_m(I_{+} - I_{-}) \tag{2.10}$$

Therefore, the behavior of the OTRA is obtained with the schematic shown in Fig. 2.14. In this figure, if the T_Z node of the second AD 844 AN is open circuited then the transresistance gain R_m is infinite ($R_m = \infty$). With the schematic shown in Fig. 2.14, the proposed circuits in chapter 4 can be implemented on laboratory bread board to check the theoretical analysis.

2.4 SUMMARY

In this chapter, the OTRA characteristics are given in detail. The ideal OTRA based terminal relations are presented along with the OTRA non-ideal model. The CMOS OTRA realizations proposed in [32, 33] are redesigned using cadence gpdk 180 nm technology. Spectre simulation models are used to simulate the CMOS OTRAs. Two CMOS OTRA realizations are presented in this chapter. The simulation results of input terminal resistance, output terminal resistance and the frequency response of the OTRA are included in this chapter. The OTRA prototype model is also presented in this chapter using two AD 844 AN ICs. This prototype model is helpful in the performance evaluation of OTRA based circuits on a laboratory breadboard.

CHAPTER 3

LITERATURE REVIEW

3.1 INTRODUCTION

Having now established some background about the operational transresistance amplifier, let us turn our attention to discuss some applications of OTRA. OTRA is one of the most important building block in the field of analogue integrated circuit. It can be used to realize different applications such as: differential integrator, differential amplifier, voltage gain amplifiers (VGAs), filters, proportional integral and derivative (PID) controllers, analogue multiplier, immitance simulators, oscillators and square/triangular waveform generator [45-89]. The input terminals of the OTRA are virtually grounded, in consequence, most of the parasitic capacitances and resistances will be disappeared. Then it is possible to obtain accurate transfer function by using OTRA in a negative feedback loop. By using OTRA, it is possible to design the applications without linear passive resistances and it is a known fact, the resistance occupies the large silicon area. The OTRA based applications like filters, differential integrator, differential amplifier and VGAs are implemented without using the passive linear resistors.

3.2 OTRA APPLICATIONS

3.2.1 DIFFERENTIAL AMPLIFIER USING OTRA

The differential amplifier using OTRA [31] with three resistors is shown in Fig. 3.1. This differential amplifier is also called as voltage controlled voltage source (VCVS).

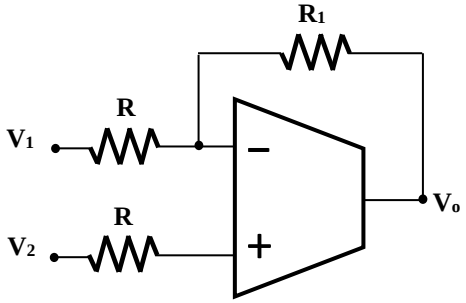


Fig. 3.1 Differential amplifier using OTRA

The output voltage of the differential amplifier circuit shown in Fig. 3.1 is given by

$$V_0 = K(V_2 - V_1) \tag{3.1}$$

where

$$K = \frac{R_1}{R}$$

The circuit in Fig. 3.1 has the advantage of providing equal gain for both inverting and non-inverting inputs, which is independent of bandwidth.

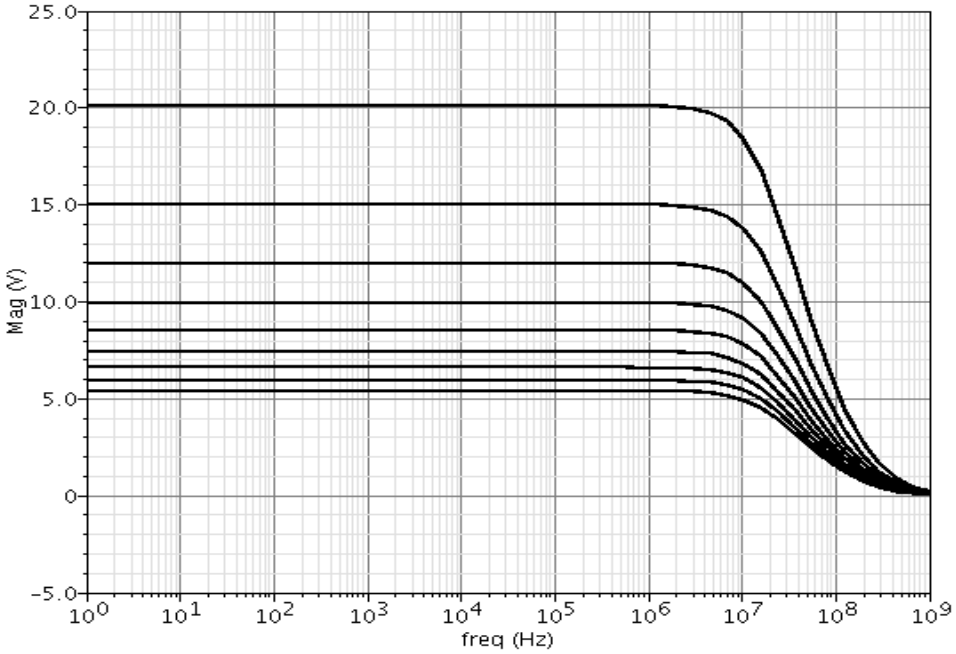


Fig. 3.2 Frequency response of the differential amplifier

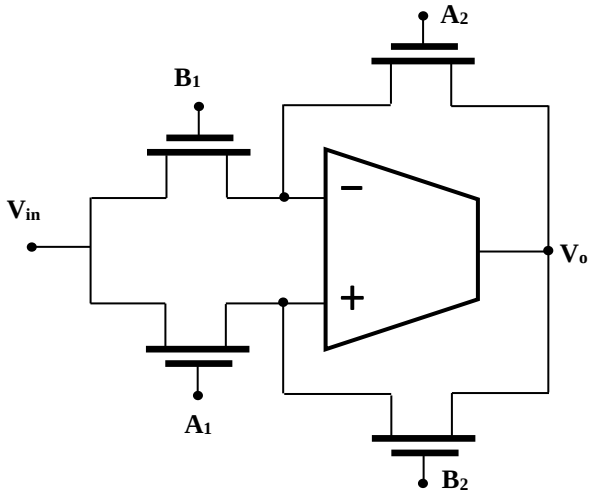


Fig. 3.3 Implementation of differential amplifier using MOS-C [31]

This property is unavailable in traditional voltage-mode (op-amp) devices. The Fig. 3.2 shows the simulation results of the circuit depicted in Fig. 3.1. The passive component values used for the simulation are R_1 is kept constant and R is varied from 1 kΩ to 10 kΩ. The circuit in Fig. 3.1 can also be implemented without using the resistors. The circuit shown in Fig. 3.3 was introduced in [31]. In this work, the application of the OTRA is implemented using MOS-resistors with the non-linearity cancellation technique. The controlled voltage applied to the gate terminal of the transistors can be used to control the conductance G. This implementation is also called as MOS-C (MOSFET and capacitors) implementation. The output voltage at V_o terminal is given by:

$$V_o = (G_1/G_2)V_i \tag{3.2}$$

where

$$G_1 = K_{N1}(V_{A1} - V_{B1}) \tag{3.3}$$

and

$$G_2 = K_{N2}(V_{A2} - V_{B2}) \tag{3.4}$$

$$K_N = \mu C_{OX}\left(\frac{W}{L}\right) \tag{3.5}$$

3.2.2 DIFFERENTIAL INTEGRATOR USING OTRA

The differential integrator circuit is shown in Fig. 3.4 with two resistors and a negative feedback capacitor [31]. The effect of stray capacitance is reduced by the virtual grounded connection of the feedback capacitor. The advantage of the proposed circuit is, it is possible to get both the positive and negative transfer function. The output voltage at terminal V_o can be given as

$$V_o = \frac{\omega_o}{s}(V_2 - V_1) \tag{3.6}$$

where

$$\omega_o = \frac{1}{RC} \tag{3.7}$$

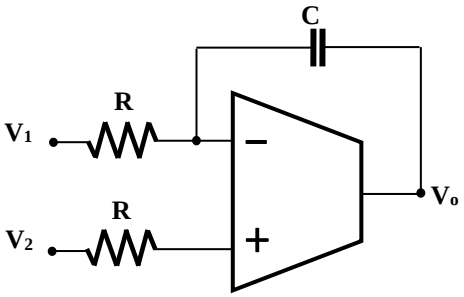


Fig. 3.4 Differential integrator using OTRA

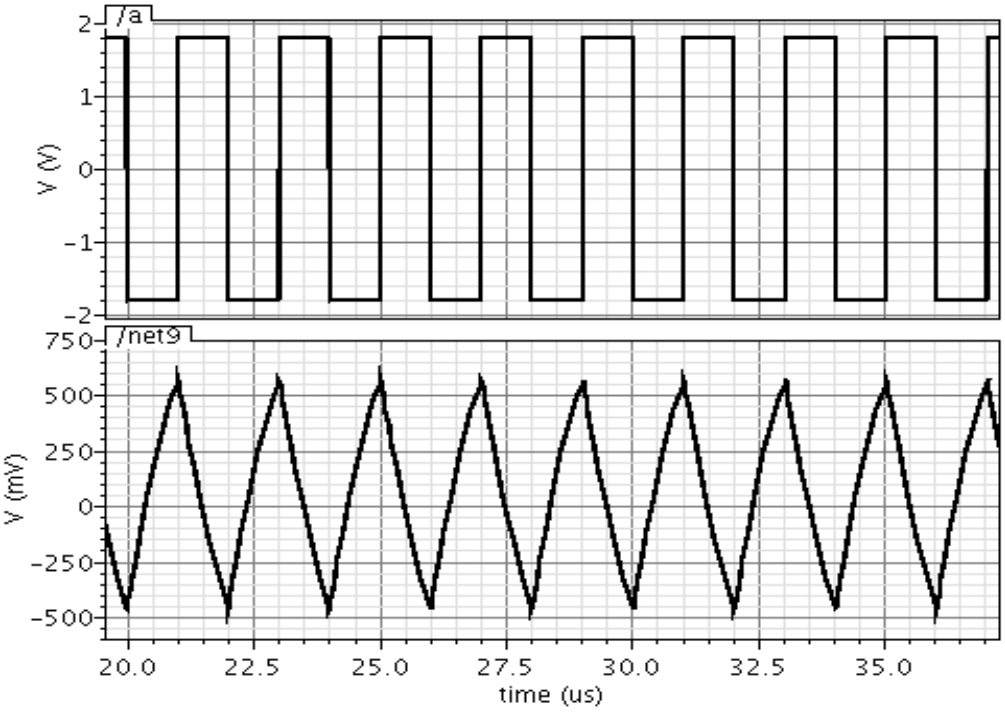


Fig. 3.5 Simulated output voltage of the differential integrator

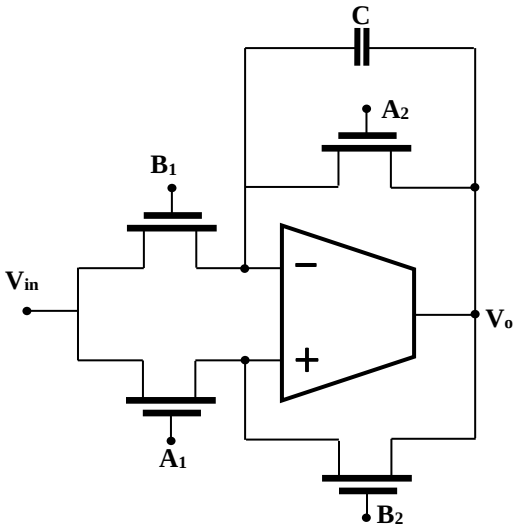


Fig. 3.6 Implementation of the OTRA differential integrator using MOS-C [31]

The transient response of the circuit in Fig. 3.4 is shown in Fig. 3.5. A feedback resistor is connected in parallel with the capacitor to solve the infinite gain problem in differential integrator circuit in Fig. 3.4. The advantage of connecting the capacitor in the feedback loop is to achieve the self compensation without any additional elements. The MOS-C implementation of the differential integrator using OTRA is shown in Fig. 3.6. The transfer function of the circuit in Fig. 3.6 is given by

$$\frac{V_o}{V_i} = \frac{G_1}{G_2} \frac{1}{\frac{s}{\omega_o} + 1} \tag{3.8}$$

Where

$$\omega_o = \frac{G_2}{C} \tag{3.9}$$

By adjusting the values of the gate voltages the differential integrator can achieve both ideal and lossy integration. The ideal integration can be done by making V_{A2} and $V_{B2} = 0$.

3.3 OTRA BASED SQUARE WAVEFORM GENERATORS

The first OTRA based square waveform generator was proposed by C. L. Hou *et al.*, [45] in the year 2005. In this work [45], two square waveform generators were proposed, these circuits consists of only one OTRA and a few external passive components.

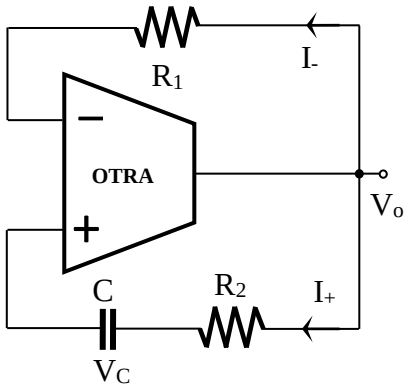


Fig. 3.7 OTRA based square waveform generator proposed in [45]

The first circuit was built with one OTRA and three passive components to produce the symmetrical square waveform with approximately fixed duty cycles and a variable frequency. The second circuit is able to control the on-duty and off-duty cycles of a square waveform independently by varying the value of the passive elements. This circuit was built with one OTRA, two diodes along with a few passive components. The first circuit with one OTRA and three passive components is shown in Fig. 3.7. The square waveform generators in [45] are simpler than the traditional voltage mode based (op-amp) waveform generators.

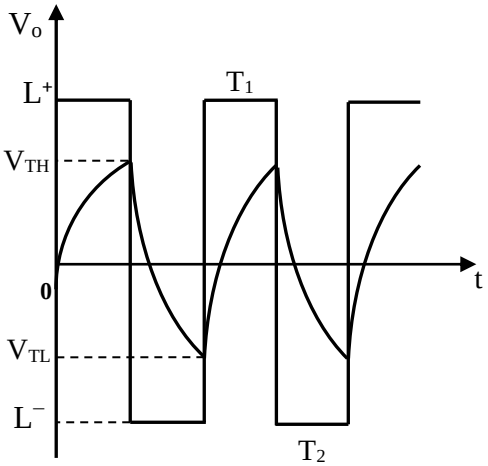


Fig. 3.8 Output waveform of the OTRA based square waveform generator in Fig. 3.7

The operation of the square waveform generator circuit in Fig. 3.7 can be explained with the help of its output waveform shown in Fig. 3.8. The output waveform in Fig. 3.8 has two saturation levels L^+ and L^-. Initially the output voltage V_o is at any one of these two saturation levels. The operation of the circuit can be explained as follows. Assume V_o is changing its state from L^- to L^+ at the time t = 0. At this time, the voltage V_C of the capacitor C starts to increase from its lower threshold value V_{TL} to its final value L^+. Where V_{TL} is the initial capacitor voltage at t = 0. In consequence, the capacitor voltage is finally charged to its upper threshold value V_{TH}, rather than L^+. When $t = T_1$, it also indicates that the current flowing into the non-inverting input terminal I_+ becomes slightly less than the inverting input terminal I_- current. So the output changes its state to the lower saturation level L^-. The upper threshold value and lower threshold value are derived from the non-inverting input terminal current I_+, inverting input terminal current I_- and from the ideal behaviour of OTRA is given in equations (3.10) and (3.11).

$$V_{TL} = \left(1 - \frac{R_2}{R_1}\right) L^- \tag{3.10}$$

$$V_{TH} = \left(1 - \frac{R_2}{R_1}\right) L^+ \tag{3.11}$$

Then the time period T_1 in Fig. 3.8 can be expressed as

$$T_1 = R_2 C \ln\left(\frac{V_{TL} - L^+}{V_{TH} - L^+}\right) \tag{3.12}$$

$$R_2 C \ln\left(\frac{2R_1}{R_2} - 1\right) = T_{on} \tag{3.13}$$

For time period T_2, the V_o remains at L^- and capacitor discharged until the non-inverting input terminal current I_+ becomes larger than inverting input terminal current I_-, when $V_C = V_{TL}$. The dynamic equation of V_C in the time period T_2 can be expressed as

$$T_2 - T_1 = R_2 C \ln\left(\frac{V_{TH} - L^-}{V_{TL} - L^-}\right) \tag{3.14}$$

$$R_2 C \ln\left(\frac{2R_1}{R_2} - 1\right) = T_{off} \tag{3.15}$$

From equations (3.14) and (3.15), for producing a square waveform in the circuit shown in Fig. 3.7, it is necessary that

$$R_1 > R_2 \tag{3.22}$$

The output square wave frequency f_o at the output terminal of the OTRA is given as

$$f_0 = \frac{1}{2R_2 C \ln\left(\frac{2R_1}{R_2} - 1\right)} \tag{3.23}$$

The on-duty and off-duty cycles of the square waveform for the Fig. 3.7 are almost fixed and it is not possible to increase or decrease the width of the duty cycles.

To eliminate this disadvantage, the second circuit was proposed in [45]. This circuit was designed with one OTRA, two diodes and four passive components. The second circuit is shown in Fig. 3.9.

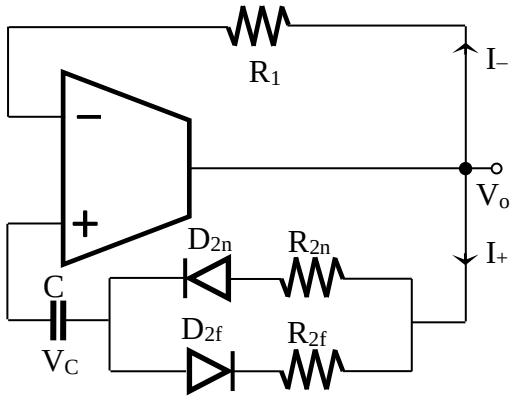


Fig. 3.9 Second proposed square waveform generator in [45]

The operation of the second proposed circuit in Fig. 3.9 is same as stated in the first proposed circuit operation. Neglecting the voltage drops of the diodes in the Fig. 3.9, the equations for the square waveform generator can be expressed as

$$T_{on} = R_2 C \ln\left(\frac{V_{TL} - L^+}{V_{TH} - L^+}\right) \tag{3.26}$$

$$R_{2n} C \ln\left(\frac{2R_1 - R_{2f}}{R_{2n}}\right) = T_{on} \tag{3.27}$$

$$T_{off} = R_{2f} C \ln\left(\frac{V_{TH} - L^-}{V_{TL} - L^-}\right) \tag{3.28}$$

$$R_{2f} C \ln\left(\frac{2R_1 - R_{2n}}{R_{2f}}\right) = T_{off} \tag{3.29}$$

$$f_o = \frac{1}{C\left(R_{2n} \ln\left(\frac{2R_1 - R_{2f}}{R_{2n}}\right) + R_{2f} \ln\left(\frac{2R_1 - R_{2n}}{R_{2f}}\right)\right)} \tag{3.30}$$

To produce a square waveform in the second proposed circuit, it is necessary to maintain

$$R_1 > R_{2n} \tag{3.31}$$

and

$$R_1 > R_{2f} \tag{3.32}$$

The on-duty (T_{on}) and off-duty (T_{off}) cycles can be varied independently by adjusting R_{2n} and R_{2f} respectively.

3.3.1 SIMULATION RESULTS

For designing the fixed duty cycle circuit shown in Fig. 3.7, the operating frequency f_o is chosen first. Then the value of resistors R_1 and R_2 is chosen. The ratio of R_1/R_2 is chosen as low as possible. The larger R_1/R_2 ratio results in a less sensitivity of the frequency variation with respect to the resistance. The capacitor value is arbitrarily chosen from the equation (3.23).

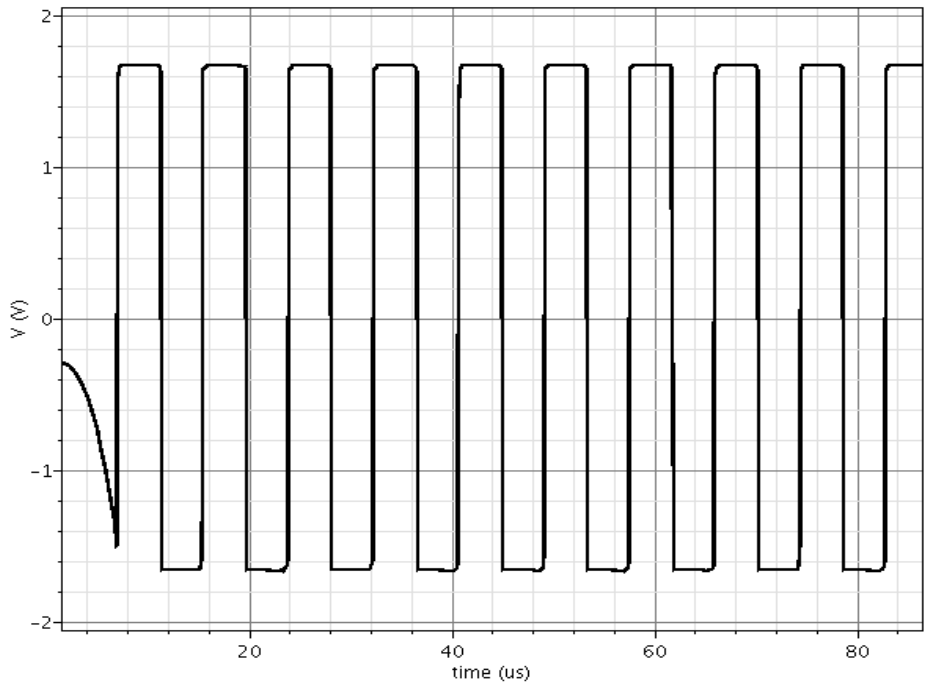


Fig. 3.10 Simulation result of the square waveform generator circuit in Fig. 3.7

For example, if f_o is chosen as 100 kHz, then the ratio of resistors R_1/R_2 is set to be 10 and C is arbitrarily chosen as 1nF. Then R_2 and R_1 can be calculated from equation (3.23) as 1.7 kΩ and 17 kΩ. If the required frequency is 100 Hz, then 1 nF capacitor is replaced by 1 µF capacitor without changing the R_1/R_2 ratio. In order to investigate the circuits proposed in [45], several experiments were performed on circuits shown in Fig. 3.7 and Fig. 3.9 at supply voltages ± 1.8 V. The Cadence Spectre simulation result for the proposed circuit in Fig. 3.7 is shown in Fig. 3.10 with

a frequency of 100 kHz. The passive components R_1 = 17 kΩ, R_2 = 1.7 kΩ and C = 1 nF were used for the simulation. For selecting the passive component values for the second circuit shown in Fig. 3.9, followed the same procedure as stated to select the passive component values in the first square waveform generator circuit. For example, if f_o is chosen as 100 kHz, the circuit parameters are selected as C = 1nF, R_1 = 17 kΩ, and $R_2 = R_{2f} = R_{2n}$ = 1.7 kΩ. The simulated output waveform for the circuit in Fig. 3.9 is shown in Fig. 3.11.

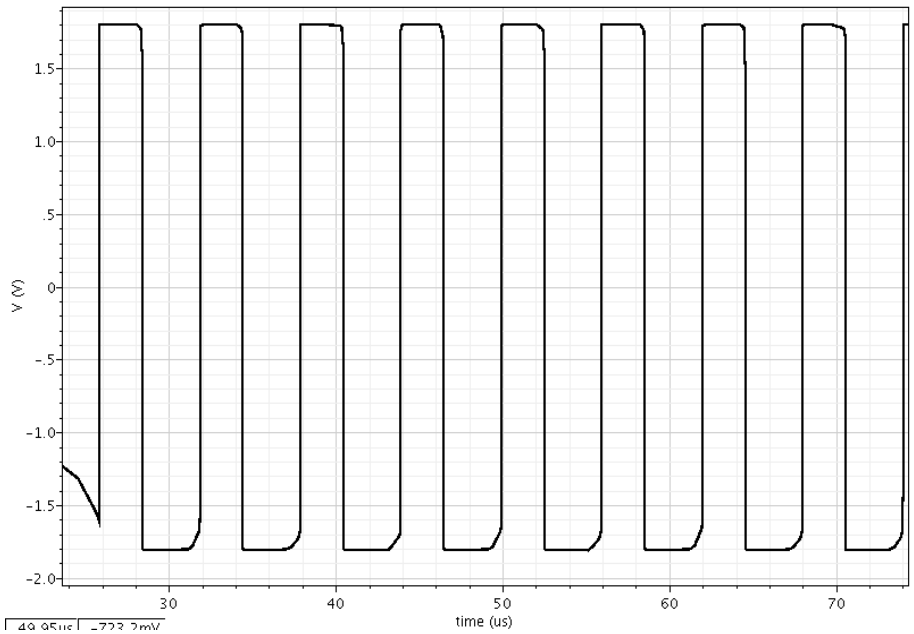


Fig. 3.11 Simulation result of the square waveform generator circuit in Fig. 3.9

The resistors R_{2f} and R_{2n} are varied independently to vary the on-duty and off-duty cycles of the output square waveform.

3.3.2 DISCUSSIONS AND CONCLUSIONS

The proposed circuits in [45] are simpler than the traditional voltage-mode square waveform generators. From Fig. 3.10, it can be seen that the on-duty and off-duty cycles are not same for the first proposed circuit in Fig. 3.7. Small percentage of error present between the on-duty and off-duty cycles. For the second circuit shown in Fig. 3.9, the capacitor value is slightly adjusted to fine tune the output square wave frequency. For the 60% on-duty cycle, R_{2n} is larger than the R_{2f}. The capacitor voltage increases to a smaller V_{TH} with an even slower charging rate in the on-period. The minimum frequency range of the square waveform circuits in Fig. 3.7 and 3.8 is

limited by the values of the passive components connected to the circuits, mainly the capacitor. Large value of capacitor makes lower output frequency.

The highest frequency at the output terminal is limited due to the slew-rate of the active device. The highest output frequency is around several MHz. However, the circuit has the advantage of less passive components, but it makes a non-linear variation of the time period with respect to the resistor R_2 and R_1 value sholud be larger than R_2 value to produce oscillations. The Fig. 3.12 shows the non-linear variation of time period with respect to the resistor R_2. For tuning the resistor R_2, passive components C = 1nF R_1 = 18kΩ were chosen and R_2 was varied from 200Ω to 18 kΩ. Moreover, the circuits proposed in [45] consume large amount of power with a supply voltage of ± 15 V.

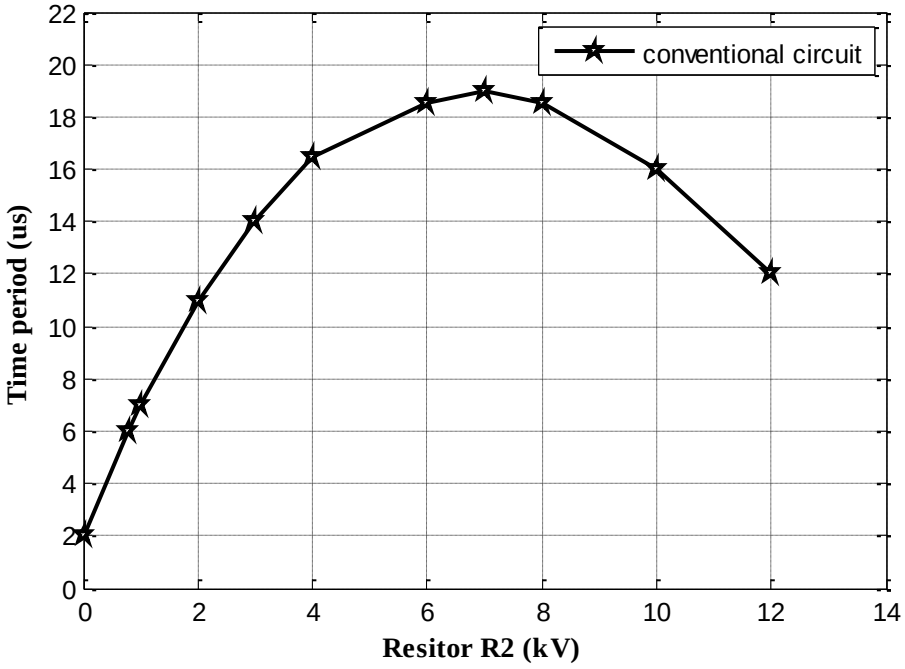


Fig. 3.12 Variation of time period for the square waveform generator circuit shown in Fig. 3.9

3.4 OTRA BASED SQUARE/TRIANGULAR WAVEFORM GENERATOR

The OTRA based square/triangle waveform generator was proposed by Y. K. Lo *et al.,* in the year 2007 [46]. The circuit was implemented with two OTRAs, three switches and a few passive components. The circuit proposed in [46] has an advantage of producing both inverting and non-inverting mode of operations. The OTRA based square/triangle waveform generator is shown in Fig. 3.13. The operation

of the circuit can be explained as follows: for inverting mode operation the switches a2 is connected to c2 and a3 is connected to b3. For non-inverting mode operation the switches are connected as; a2 is connected b2 and a3 is connected to c3. The expected output waveform is shown in Fig. 3.14.

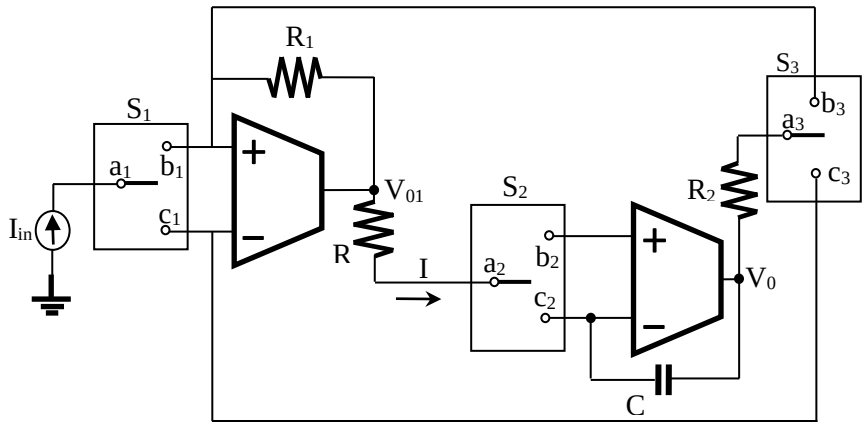


Fig. 3.13 OTRA based square/triangle waveform generator

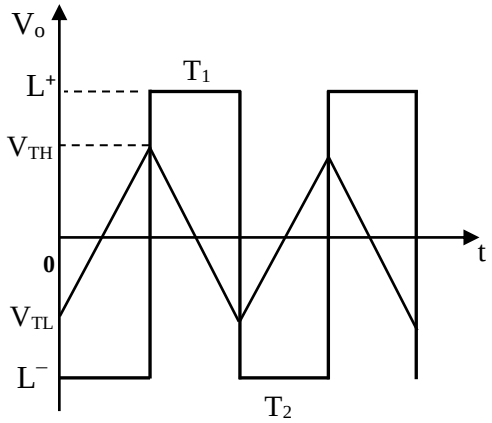


Fig. 3.14 Expected output waveform from the circuit in Fig. 3.13

From the Fig. 3.14, the output is at negative saturation level L^-. The saturation current I, flows through the resistor R and C, this makes V_{02} to increase linearly.

$$I = \frac{V_{01}(t)}{R} = \frac{L^-}{R} = C\frac{dV_{02}}{dt} \tag{3.33}$$

This state continues until V_{02} reaches the upper threshold voltages $V_{TH.}$ The upper threshold voltage can be derived by making inverting and non-inverting currents equal.

$$V_{TH} = R_2 I_{in} + \frac{R_2}{R_1} L^+ \tag{3.34}$$

When a1 is connected to b1,

$$V_{TH} = -R_2 I_{in} + \frac{R_2}{R_1} L^+ \tag{3.35}$$

Similarly, for lower threshold voltage V_{TL},

$$V_{TL} = R_2 I_{in} - \frac{R_2}{R_1} L^+ \tag{3.36}$$

$$V_{TL} = -R_2 I_{in} - \frac{R_2}{R_1} L^+ \tag{3.37}$$

The on-duty and off-duty cycles time period can be derived from the equations (3.34)-(3.37).

$$T_1 = 2RC \frac{R_2}{R_1} \tag{3.38}$$

and for off-duty cycle,

$$T_2 = 2RC \frac{R_2}{R_1} = T_{off} \tag{3.39}$$

The oscillation frequency is given by,

$$f = \frac{1}{4RC\left(\frac{R_2}{R_1}\right)} \tag{3.40}$$

3.4.1 SIMULATION RESULTS

The circuit shown in Fig. 3.13 was simulated using Cadence Spectre simulation model parameters. The simulated square/triangular waveform is shown in Fig. 3.15.

3.4.2 DISCUSSIONS AND CONCLUSIONS

The equation (3.40) is useful to facilitate the design of square/triangular waveform generator shown in Fig. 3.13. The oscillation frequency is specified first, and then the ratio R_2/R_1 is found from equation (3.40) for an arbitrarily chosen capacitor C and resistor R values. The circuit has an advantage of producing both inverting and non-inverting output waveforms. The circuit presented in [46] is

successfully eliminated the errors presented in voltage-mode square/triangle waveform generator, specifically frequency and amplitude are dependent.

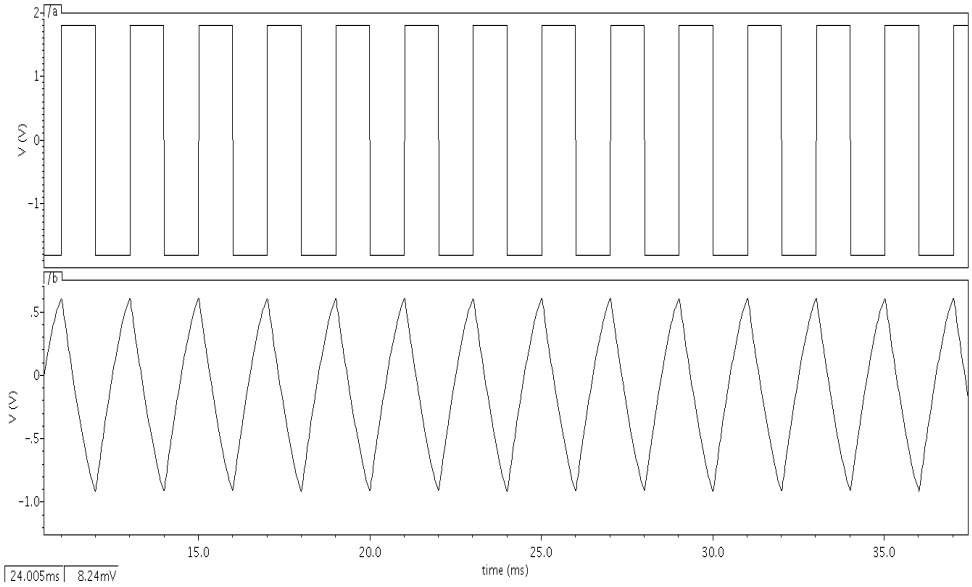


Fig. 3.15 Simulated output waveform from the circuit in Fig. 3.13

The minimum and maximum frequency range of the circuit is from kHz to few MHz. The minimum frequency is limited by the capacitor value and the maximum frequency is limited by the slew rate of the OTRA. However, the circuit shown in Fig. 3.13 is complex with three switches, two OTRAs and four passive components. Moreover, the circuit requires external current source I to adjust the DC level of the output waveform. The operation of the circuit is also complex with the switching positions of three switches. The circuit consume high power to operate with two OTRAs, three switches and four passive components.

3.5 OTRA BASED SINUSOIDAL OSCILLATORS

The first OTRA based sinusoidal waveform generator was proposed by K. N. Salama *et al.,* in the year 2000 [50]. Seven new sinusoidal oscillator designs are reported in [50]. In this paper, three oscillator circuits are realized from a generalized configuration using single OTRA and four sinusoidal oscillator circuits are designed using two OTRAs with a few passive components. The generalized configuration to realise several sinusoidal oscillators using single OTRA is shown in Fig. 3.16.

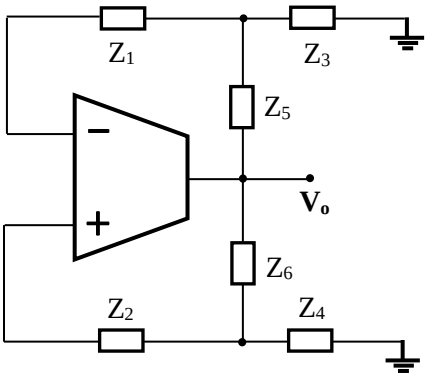


Fig. 3.16 OTRA based generalized configuration.

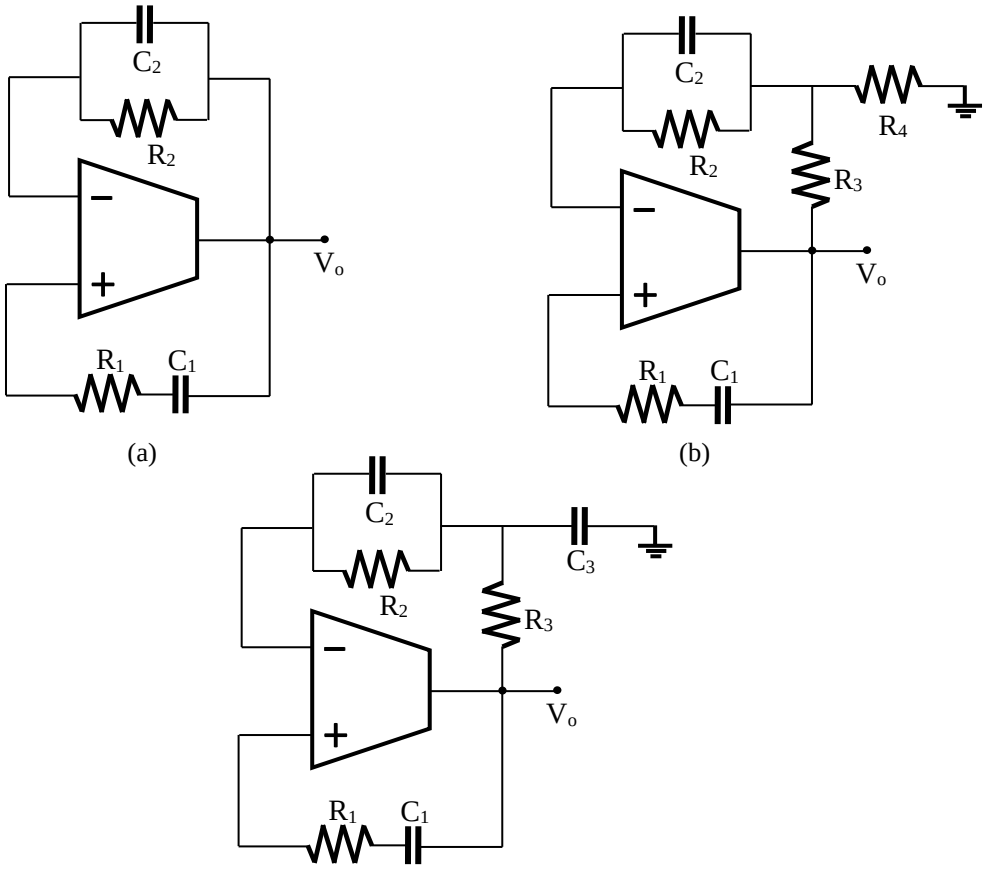


Fig. 3.17 Oscillators realized from the generalized configuration in Fig. 3.16

Assuming the OTRA used in the generalized configuration is ideal; the characteristic equation for the generalized configuration is by:

$$Z_2 + Z_5\left(1+\frac{Z_2}{Z_3}\right) = Z_1 + Z_6\left(1+\frac{Z_1}{Z_4}\right) \tag{3.41}$$

Several oscillator circuits can be realized from the generalized configuration. Three special cases are shown in the Fig. 3.17. Minimum passive component oscillator that can be realized from the generalized configuration is show in Fig. 3.17 (a). The circuit shown in Fig. 3.17 (a) requires two capacitors and two resistors to produce the oscillation. The condition of oscillation and frequency of oscillation are given by

$$\frac{R_1}{R_2}+\frac{C_2}{C_1}=1 \tag{3.42}$$

$$\omega_o=\frac{1}{\sqrt{C_1C_2R_1R_2}} \tag{3.43}$$

From equations (3.42) and (3.43), it is clear that the condition of oscillation and frequency of oscillation cannot be controlled independently from the circuit in Fig. 3.17 (a). The oscillator circuits shown in Fig. 3.17 (b) & (c) are able to control the condition of oscillation and frequency of oscillation independently. The characteristic equations for the circuits shown in Fig. 3.17 (b) & (c) can be derived from the generalized equation (3.41). For the oscillator circuit in Fig. 3.17 (b), the grounded resistor R_4 is used to control the condition of oscillation without affecting the frequency of oscillation. From the equations (3.46) and (3.47), the capacitor C_3 in Fig. 3.17 (c) is used to control the frequency without affecting the condition of oscillation. Four quadrature oscillators using two OTRAs are shown in Fig. 3.18 [50].

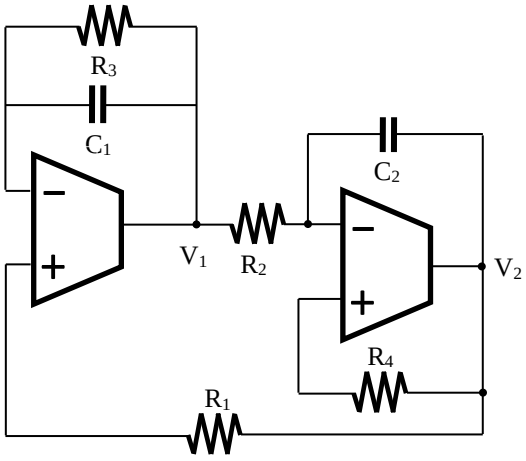
For Fig. 3.17 (b)

$$\frac{R_1}{R_2}+\frac{C_2}{C_1}=1+\frac{R_3}{R_2}+\frac{R_3}{R_4} \tag{3.44}$$

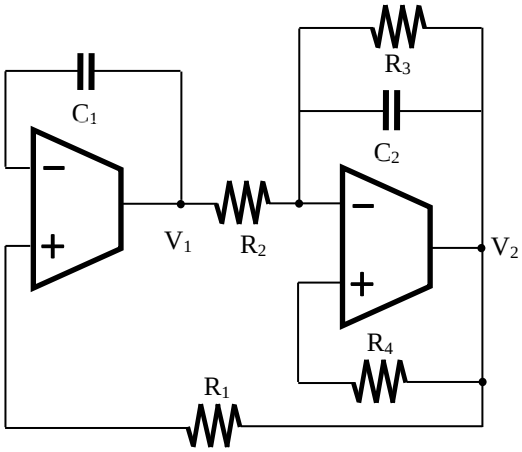
$$\omega_o=\frac{1}{\sqrt{C_1C_2R_1R_2\left(1-\frac{R_3}{R_1}\right)}} \tag{3.45}$$

For Fig. 3.17(c)

$$\frac{R_1}{R_2}+\frac{C_2}{C_1}=1+\frac{R_3}{R_2} \tag{3.46}$$



(a)



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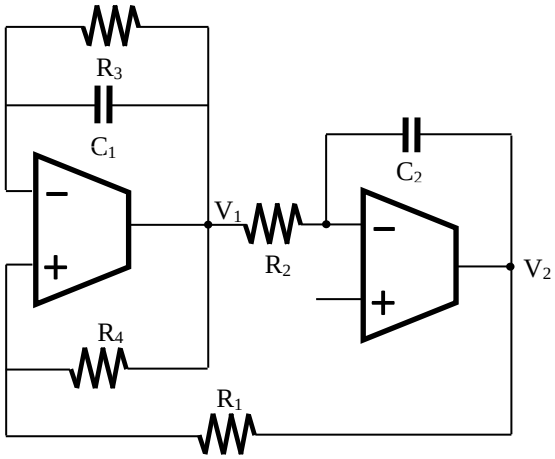
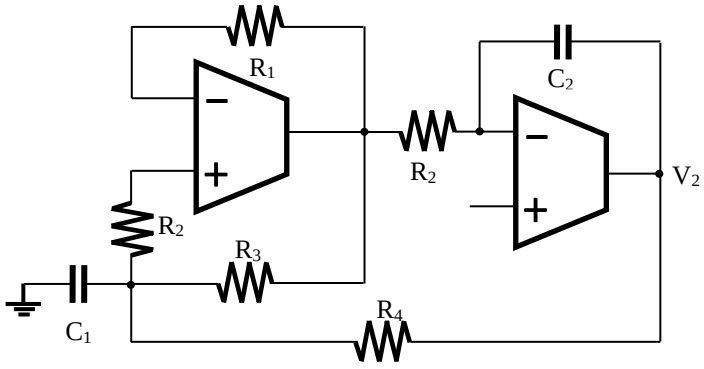


(c)



(d)

Fig. 3.18 Sinusoidal oscillators using two OTRAs

$$\omega_o = \frac{1}{\sqrt{C_1 C_2 R_1 R_2 \left(1 - \frac{R_3}{R_1}\left(1 + \frac{C_3}{C_2}\right)\right)}} \tag{3.47}$$

These oscillator circuits are constructed with two capacitors and four or five resistors. All the circuits shown in Fig. 3.18 are able to control the frequency of oscillation and condition of oscillation independently. The condition of oscillation and frequency of oscillation for these circuits are derived from the state matrix of the corresponding circuits.

$$C_1 R_3 = C_2 R_4 \tag{3.48}$$

$$\omega_o = \frac{1}{\sqrt{C_1 C_2 R_1 R_2 \left(1 - \frac{R_1 R_2}{R_3 R_4}\right)}} \tag{3.49}$$

The equations (3.48) and (3.49) are derived from the state matrix shown below for the circuit in Fig. 3.18 (a).

$$\begin{bmatrix} \frac{dV_1}{dt} \\ \frac{dV_2}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{C_1 R_3} & \frac{1}{C_1 R_1} \\ -\frac{C_2}{R_2} & \frac{1}{C_2 R_4} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{3.50}$$

The condition of oscillation and frequency of oscillation is same for the circuits in Figs. 3.18 (b) and (c).

$$R_3 = R_4 \tag{3.51}$$

$$\omega_o = \frac{1}{\sqrt{C_1 C_2 R_1 R_2}} \tag{3.52}$$

For producing oscillations in the circuit shown in Fig. 3.18 (d), it requires, two OTRAs, four resistors and two capacitors. The condition of oscillation and frequency of oscillation is given in equations (3.53) and (3.54).

$$R_3 = 3R \tag{3.53}$$

$$\omega_o = \frac{3}{\sqrt{C_1 C_2 R_1 R_2}} \tag{3.54}$$

A novel single resistance controlled sinusoidal oscillator employing single OTRA was proposed by U. Cam in the year 2002 [51]. The circuit proposed in [51] is simpler than the circuits in Fig. 3.17.

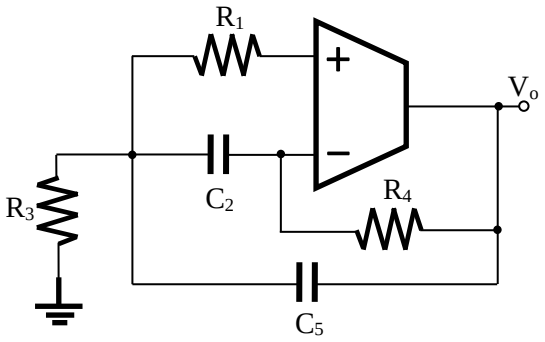


Fig. 3.19 SRCO using single OTRA

The circuit diagram of the oscillator is shown in Fig. 3.19. Routine analysis for the above circuit gives the following equations.

$$C_2G_4 + C_5G_4 = C_5G_1 \tag{3.55}$$

$$f = \frac{1}{2\pi}\sqrt{\frac{G_4(G_1+G_3)}{C_2C_5}} \tag{3.56}$$

Form the above equations (3.55) and (3.56), it is clear that the grounded resistor R_3 is used to control the frequency of the oscillator without disturbing the condition of oscillation. This oscillator is also called as single resistance controlled oscillator (SRCO). Minimum component oscillator along with one SRCO and one single capacitance controlled oscillator (SCCO) were proposed in [52]. The circuits reported in [52] are shown in Fig. 3.20. The minimum component oscillator is shown in Fig. 3.20 (a). This oscillator circuit requires two capacitors and two resistors to produce the oscillation. However, it is not possible to control the condition of oscillation and frequency of oscillation independently with the minimum component circuit in Fig. 3.20 (a). The mathematical equations derived from the above circuits are given in the below equations. For Fig. 3.20 (a)

$$\frac{G_2}{G_1} - 1 = \frac{C_2}{C_1} \tag{3.57}$$

$$\omega_o = \sqrt{\frac{G_1 G_2}{C_1 C_2}} \tag{3.58}$$

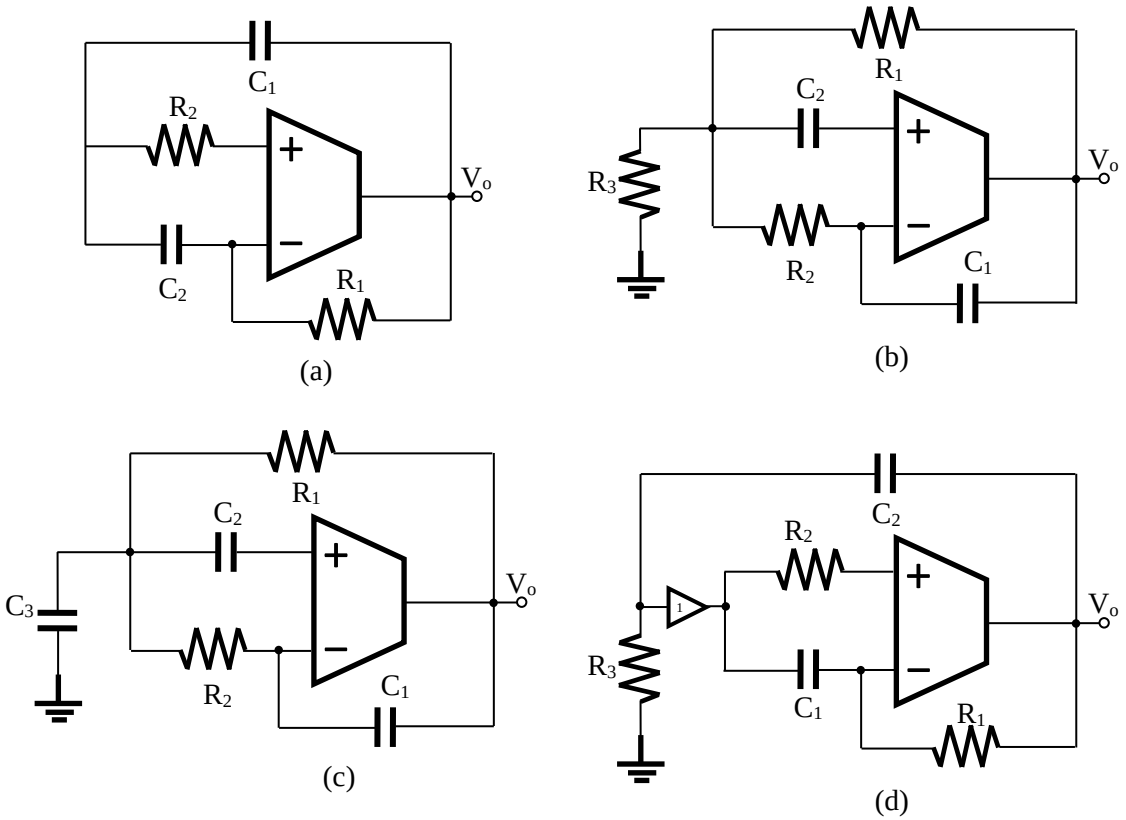


Fig. 3.20 Minimum component, SRCO and SCCO oscillators using single OTRA

For Fig. 3.20 (b)

$$1 + \frac{G_2}{G_1} + \frac{G_3}{G_1} = \frac{C_2}{C_1} \tag{3.59}$$

$$\omega_o = \sqrt{\frac{G_1 G_2}{C_1 C_2}} \tag{3.60}$$

For Fig. 3.20 (c)

$$1 + \frac{G_2}{G_1} = \frac{C_2}{C_1} \tag{3.61}$$

$$\omega_o = \sqrt{\frac{G_1 G_2}{C_1 (C_2 + C_3)}} \tag{3.62}$$

The oscillator circuits shown in Fig. 3.20 (b) & (c) are able to control the oscillation condition and the frequency of oscillation independently and the same is proven from the equations (3.59)-(3.62). The circuit shown in Fig. 3.20 (d) was proposed by Ashish G. *et al.*, in the year 2012 [53]. Two grounded resistance/capacitance (SRCO/SCCO) oscillators were reported in [53], the first oscillator circuit [53] with a grounded capacitor is similar to the circuit shown in Fig. 3.19 (c). These oscillator circuits can also be used as grounded inductance simulators by removing the grounded passive components and applying input current to the buffer. The condition of oscillation and frequency of oscillation derived from the circuit in Fig. 3.19 (d) is given in equations (3.63) and (3.64).

$$R_2 \leq R_1 \tag{3.63}$$

$$f = \frac{1}{2\pi\sqrt{R_1 R_3 C_1 C_2}} \tag{3.64}$$

3.5.1 SIMULATION RESULTS

All the circuits shown in Figs. 3.17, 3.18, 3.19 and 3.20 were simulated using Cadence Spectre simulation model parameters. The simulation result for the circuit in Fig. 3.17 (a) is shown in Fig. 3.21. The passive components R_1 =10 kΩ, R_2 = 20 kΩ, C_1 =10 nF and C_2 =15 nF were used for the simulation with a supply voltage of ± 1.8 V.

3.5.2 DISCUSSIONS AND CONCLUSIONS

The oscillator circuits shown Figs 3.17, 3.18, 3.19 and 3.20 are able to produce sinusoidal waveforms from a few kHz to several MHz. The circuits shown in Fig. 3.17 (a) and 3.20 (a) are minimum component oscillators. The advantages of these two circuits are less in number of passive components and single OTRA. However, all the passive components used in these two circuits are floating and it is hard to fabricate the integrated circuit (IC) with all floating passive components. The generalized configuration shown in Fig. 3.16 is used to realize only few oscillator circuits. The frequency spectrum is also given for the circuit in Fig. 3.17 (a). The oscillator circuits generated from the generalized configuration require more number of passive components. The oscillator circuits realized from the generalized configuration are shown in Fig. 3.17 (b) & (c).

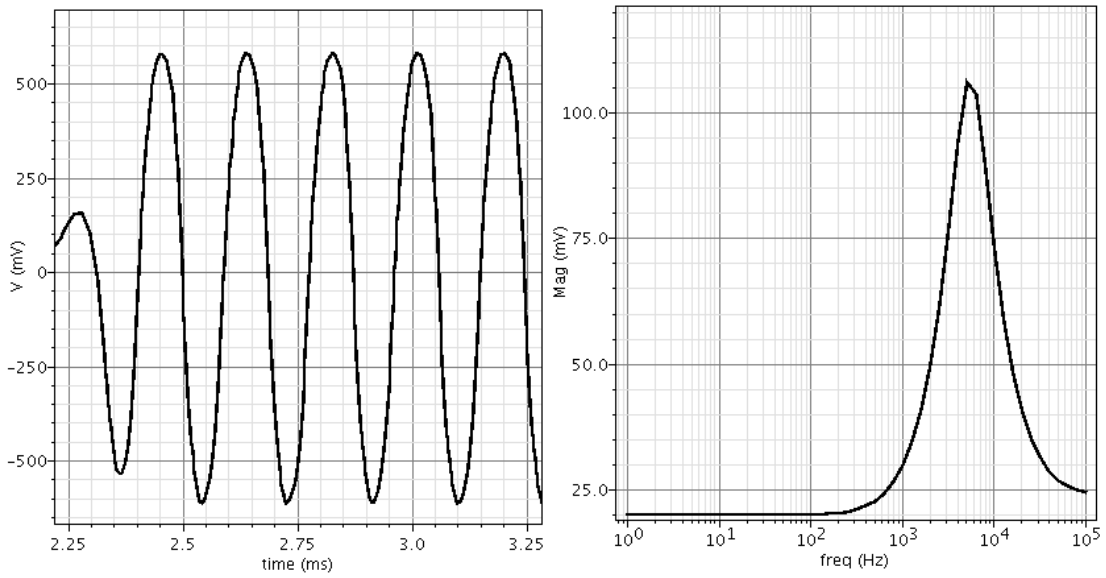


Fig. 3.21 Simulation result for the oscillator circuit shown in Fig. 3.17 (a)

These two oscillator circuits require six passive components to generate the oscillations. However, these circuits have grounded passive components, but, more passive component occupies greater chip area in IC fabrication. The oscillator circuits shown in Figs. 3.18(a), (b) and (c) are quadrature sinusoidal oscillators. These quadrature oscillators produce two sinusoidal outputs with 90^o phase difference between them. The oscillator circuit shown Fig. 3.18 (d) requires two OTRAs and seven passive components. This oscillator circuit consumes high power to produce the oscillation. A similar circuit with two OTRAs and three resistors and three capacitors is reported in [64]. This circuit also consumes a high amount of power to produce the oscillations.

3.6 SUMMARY

A brief on existing OTRA based waveform generators available in the literature is presented in this chapter. The circuits given in this chapter are redesigned using Cadence gpdk 180 nm and simulated using Spectre simulation model parameters. A few OTRA applications are also included in this chapter. The working of OTRA based circuits such as sinusoidal oscillators, square waveform generators and square/triangular waveform generator is given in brief. The disadvantages detected during the simulation and hardware implementation of the existing OTRA based circuits are presented as intermediate conclusions in the subtopics of this chapter.

CHAPTER 4

NEW OTRA BASED WAVEFORM GENERATORS

4.1 INTRODUCTION

Sinusoidal/square wave generator circuits are the most important building blocks in the design of analogue and digital integrated circuits. These waveform generators find many applications in communication, instrumentation and measurement, and control systems. Sinusoidal/square waveform generators along with other circuits are often employed to produce various standard signals, such as triangular wave, pulse wave, square, saw tooth etc. [1-3]. These signals can be used as a test signal for the automatic test and measurement, a local oscillator for frequency translation, clock pulses for digital circuits and also in audio and speech processing. Moreover, the generated signals with phase noise become the most important in frequency domain for the radio frequency (RF) applications.

Signal generator or oscillators can be classified as

i) Sinusoidal/linear/harmonic oscillators

ii) Non-sinusoidal/non-linear/relaxation oscillator

This chapter is devoted to the realization of some novel active circuits by using an operational transresistance amplifier (OTRA). At first, the discussion begins with the realization of novel sinusoidal oscillator circuits based on a generalized configuration which is followed by two novel quadrature sinusoidal oscillator realizations. At last, the chapter ends with the design description of two new square-wave generators based on single OTRA.

4.2 SINUSOIDAL OSCILLATORS USING SINGLE OTRA

Sinusoidal oscillators are essential parts in many electronic systems. It can be used in testing, instrumentation and telecommunication systems. An electronic device that generates sinusoidal oscillations of desired frequency is known as sinusoidal oscillator. The period or frequency of the oscillator is determined by the external circuitry. Most of the oscillators can be viewed as feedback circuits, where part of the output signal is ‘feedback’ to the input signal. The functional block diagram of the sinusoidal oscillator with positive feedback is shown in Fig. 4.1.

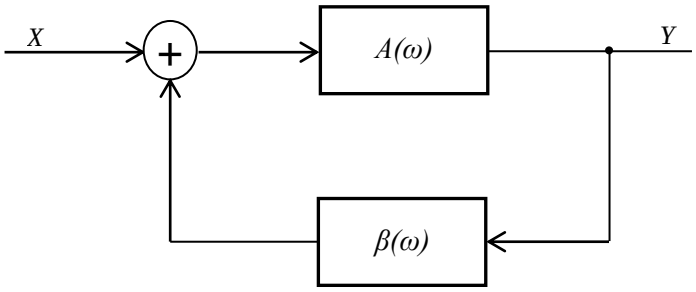


Fig. 4.1 Functional block diagram of a sinusoidal oscillator

A(ω) and β(ω) are the gains of the amplifier and frequency selective feedback network respectively. *X* and *Y* are the input and output signals. The closed loop transfer function of the block diagram shown in Fig. 4.1 becomes

$$\frac{Y}{X} = \frac{A(\omega)}{1 - A(\omega)\beta(\omega)} \tag{4.1}$$

From equation (4.1), the characteristic equation can be written as

$$1 - A(\omega)\beta(\omega) = 0 \tag{4.2}$$

According to the Barkhausen criterion, the system will sustain steady-state oscillations at a specific frequency only when the open-loop gain is equal to unity $A(\omega)\beta(\omega) = 1$. At this condition, the closed-loop gain becomes infinite and produces a finite output for the zero input signals. The Barkhausen criterion is widely used in the design of electronic oscillators and also in the design of the feedback circuits to prevent them from oscillations. All the proposed sinusoidal oscillator circuits in the following subsections satisfied the Barkhausen criterion.

4.2.1 GROUNDED RESISTANCE/CAPACITANCE SINUSOIDAL OSCILLATORS

In the previous chapters, some sinusoidal oscillators based on OTRA with some disadvantages were discussed. However, during the study of the sinusoidal oscillator circuits available in the literature, it was found that a generalized configuration can be implemented to generate more number of sinusoidal oscillators with a grounded resistance or capacitance. The proposed generalized configuration for generating sinusoidal oscillator is shown in Fig. 4.2.

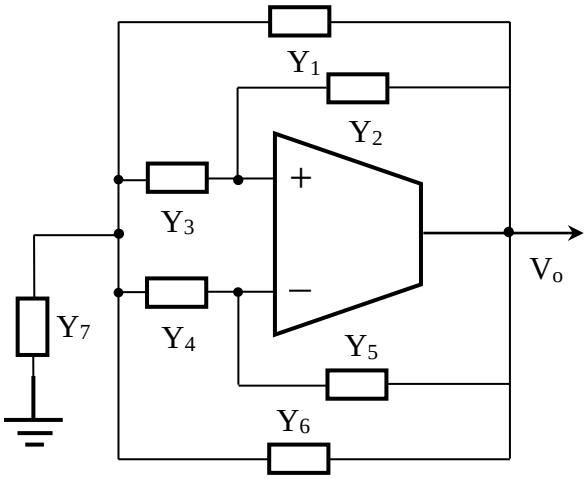


Fig. 4.2 Generalized configuration of the Single OTRA based sinusoidal oscillators

Several oscillator circuits can be generated by exploiting the generalized configuration shown in Fig. 4.2. By substituting the resistors and capacitors in place of Y_i (where i = 1 to 7) several oscillator circuits can be realized. The minimum component oscillator circuit generated from the generalized configuration is shown in Fig. 4.3.

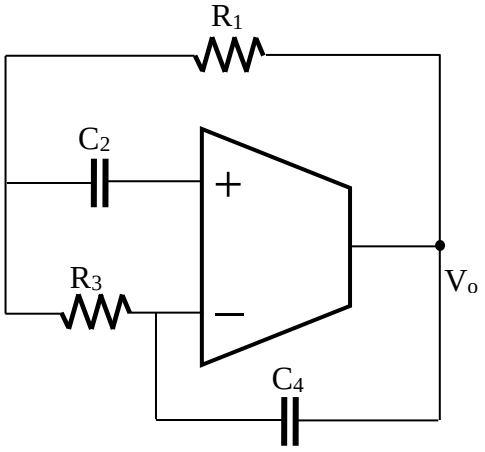


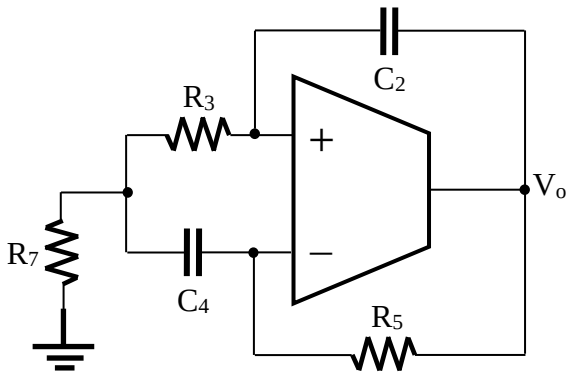
Fig. 4.3 Minimum component RC sinusoidal oscillator

The oscillator circuit shown in Fig. 4.3 can also be called as minimum passive component RC sinusoidal oscillator circuits. The admittance values chosen for the Fig. 4.3 are $Y_1 = G_1$, $Y_2 = 0$, $Y_3 = sC_2$, $Y_4 = G_3$, $Y_5 = sC_4$, $Y_6 = 0$ *and* $Y_7 = 0$. This circuit generates oscillations with two resistors, two capacitors and one OTRA. By proper selection of the admittances Y_1, Y_2, Y_3, Y_4, Y_5, Y_6 and Y_7 of the generalized configuration shown in Fig. 4.2, many oscillator circuits can be realized. Some-of the

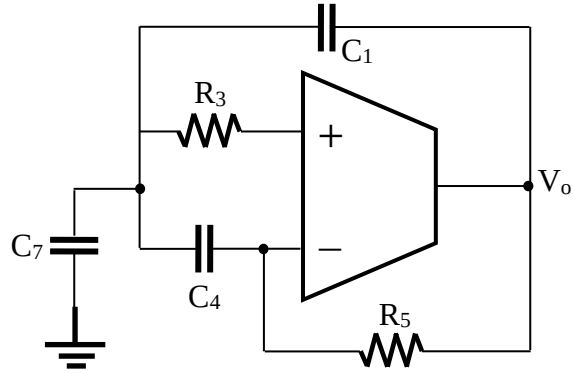
useful oscillator circuits generated from the generalized configuration with the admittances shown in Table. 4.1 are shown in Fig. 4. 4

Table. 4.1 Selected passive components for the generalized configuration shown in 4.2

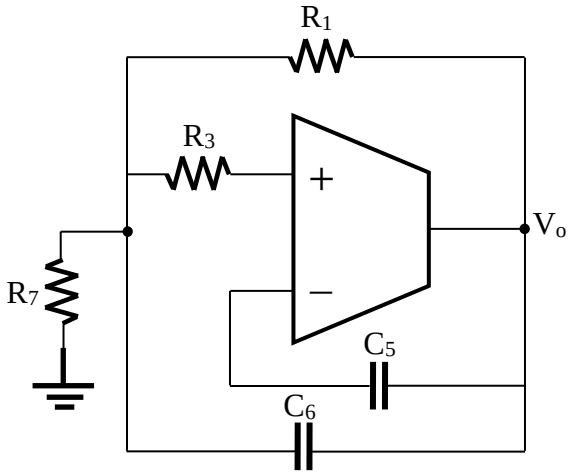
Proposed designs	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
(a)	0	sC_2	R_3	sC_4	R_5	0	R_7
(b)	sC_1	0	R_3	sC_4	R_5	0	sC_7
(c)	R_1	0	R_3	0	sC_5	sC_6	R_7
(d)	0	R_2	R_3	sC_4	R_5	sC_6	R_7
(e)	0	R_2	sC_3	R_4	0	sC_6	R_7
(f)	0	sC_2	R_3	sC_4	R_5	R_6	R_7
(g)	0	sC_2	R_3	sC_4	0	R_6	R_7
(h)	sC_1	R_2	sC_3	R_4	R_5	0	0
(i)	sC_1	sC_2	R_3	R_4	R_5	0	0
Y_i's are admittance of passive components							



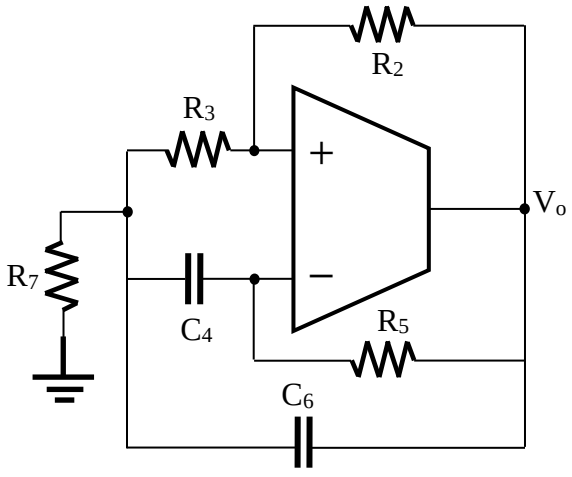
(a) Proposed oscillator circuit-I



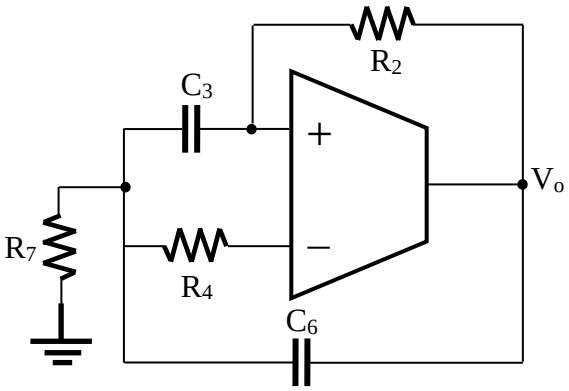
(b) Proposed oscillator circuit-II



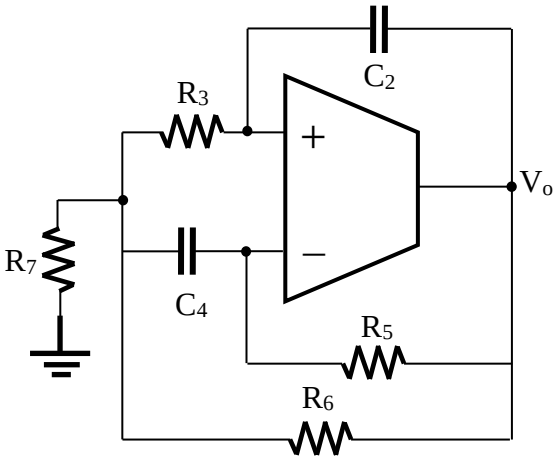
(c) Proposed oscillator circuit-III



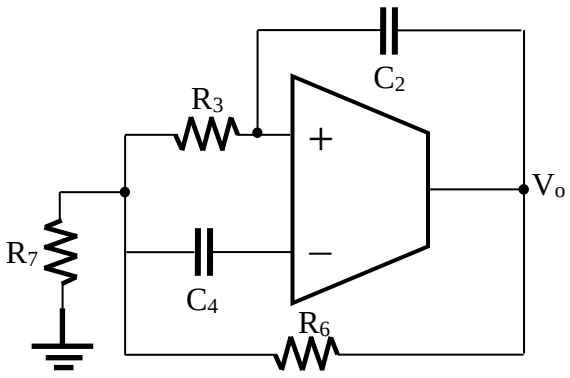
(d) Proposed oscillator circuit-IV



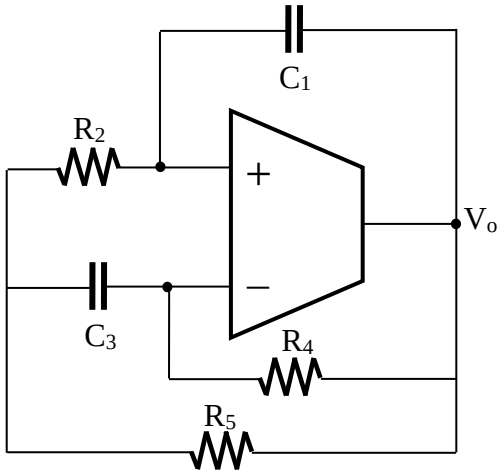
(e) Proposed oscillator circuit-V



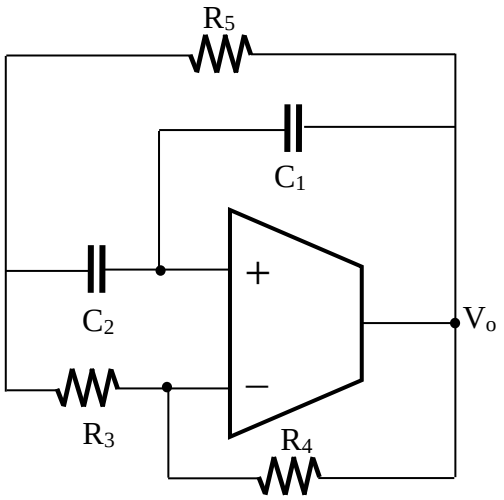
(f) Proposed oscillator circuit-VI



(g) Proposed oscillator circuit-VII



(h) Proposed oscillator circuit-VIII

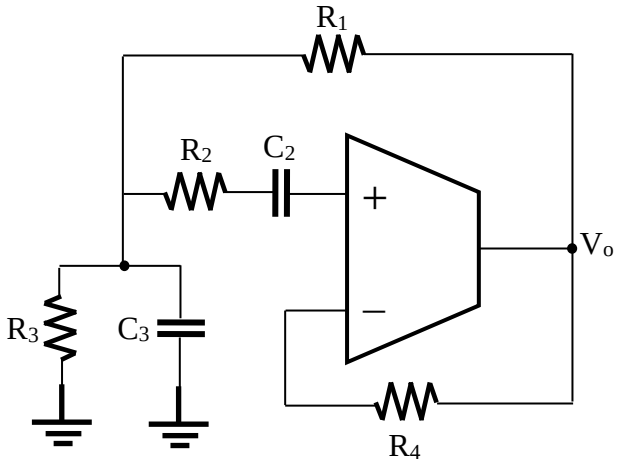


(i) Proposed oscillator circuit-IX

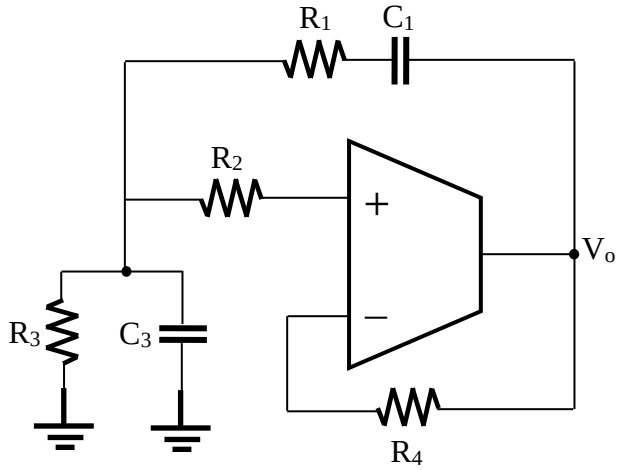
Fig. 4.4 Oscillator circuits realized from the generalized configuration

The advantage of the proposed circuits in Fig. 4.4 is a grounded resistance R_7, which can be replaced with a grounded capacitor or a JFET (Junction Field Effect Transistor) to realize a voltage controlled oscillator. Two grounded passive component oscillators can also be derived from the generalized configuration shown in Fig. 4.2. The proposed resistance and capacitance grounded sinusoidal oscillators are shown in Fig. 4.5 (a) and (b).

The proposed resistance and capacitance grounded sinusoidal oscillator circuits require single OTRA and six passive components to generate the oscillations.



(a) Grounded resistance and capacitance oscillator-I



(b) Grounded resistance and capacitance oscillator-II

Fig. 4.5 Grounded resistance and capacitance sinusoidal oscillators

4.3 QUADRATURE SINUSOIDAL OSCILLATORS

Quadrature oscillator is an important building block for many electronics and communication applications. A quadrature oscillator typically provides two sinusoids with a 90^o phase difference, which is useful in telecommunications for quadrature mixer, in single-sideband generators, in direct-conversion receivers, used for measurement purposes in vector generators or selective voltmeters.

The principle of quadrature generation is to couple two oscillators and injecting a portion of each oscillators output with the same frequency into other oscillator, such that they operate with a 90^o phase shift. Quadrature oscillators can be designed as either second order or third order oscillators. The major advantage of the second order

oscillators is compact realization with less number of passive components and active components.

4.3.1 PROPOSED QUADRATURE OSCILLATOR CIRCUITS

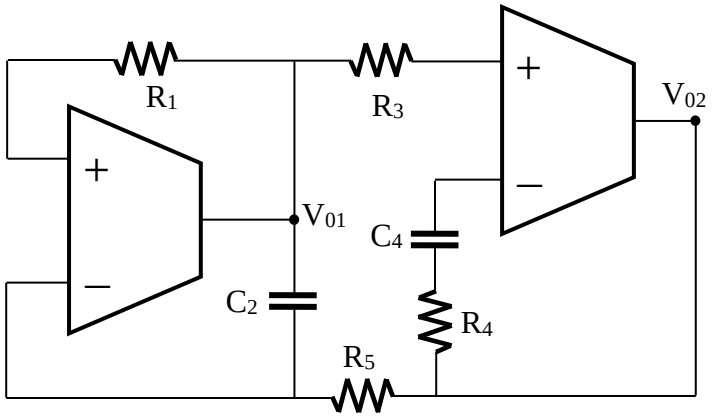


Fig. 4.6 Proposed quadrature sinusoidal oscillator circuit-I

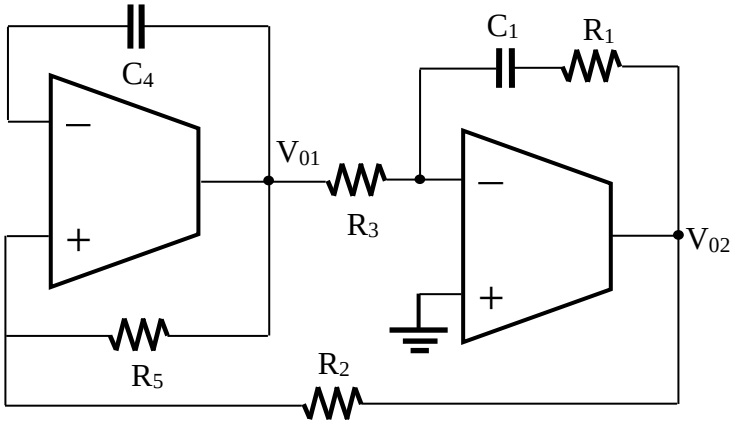


Fig. 4.7 Proposed quadrature sinusoidal oscillator circuit-II

The proposed quadrature sinusoidal oscillators are shown in Fig. 4.6 and Fig. 4.7. These quadrature oscillators require two OTRAs and few passive components to generate the oscillations with 90^{o} phase shift.

4.4 SQUARE WAVEFORM GENERATORS

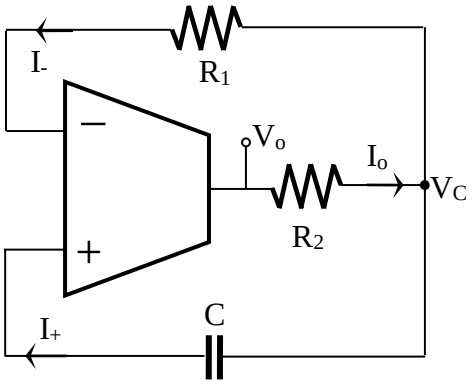
A square waveform is a kind of non-sinusoidal waveform, most commonly used in electronics and signal processing applications. An ideal square wave alternates regularly and instantaneously between two saturation levels. Square waves are usually encountered in digital switching circuits for triggering synchronous logic circuits at

precisely determined logic intervals. They are used as timing references or clock signals, because of their fast transitions between bollen logic levels (1's and 0's). Square waveform generators along with other circuits are able to generate triangular, saw-tooth and pulse waveforms.

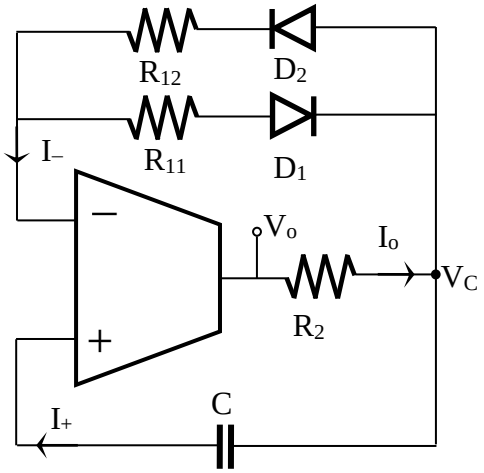
4.4.1 PROPOSED SQUARE WAVEFORM GENERATOR CIRCUITS

The proposed square wave generators are shown in Fig. 4.8. The first proposed circuit in Fig. 4.8 (a) is designed with one OTRA, and a few passive components. This circuit shown in Fig. 4.8 (a) can be able to produce the square waveform with almost equal and fixed on-duty and off-duty cycles. The proposed circuit in Fig. 4.8 (b) is to contrive by using one OTRA, two diodes and a few passive components. The second proposed circuit in Fig. 4.8 (b) is adroit to vary on-duty and off-duty cycles independently. The working principle of the proposed circuits can be explained with the expected output waveform shown in Fig. 4.9.

From Fig. 4.9, it could be construed that the output square-wave (V_o) has two saturation levels V_{sat}^{+} and V_{sat}^{-}. Assuming initially, V_o is at any one of these two saturation levels. If the output voltage V_o is at negative saturation level V_{sat}^{-} and changing it's state from V_{sat}^{-} to V_{sat}^{+}, which indicates that the current at the non-inverting terminal I_+ becomes more than the current at the inverting terminal I_- of the OTRA. At this moment, the voltage V_C of the capacitor C starts to increase from the lower threshold value V_{TL} to the final value V_{sat}^{+}. At the end of on-duty cycle, the capacitor voltage V_C is charged up to the upper threshold voltage V_{TH}, instead of V_{sat}^{+}.



(a) Square waveform generator-I



(b) Square waveform generator-II

Fig. 4.8 Proposed square waveform generator circuits

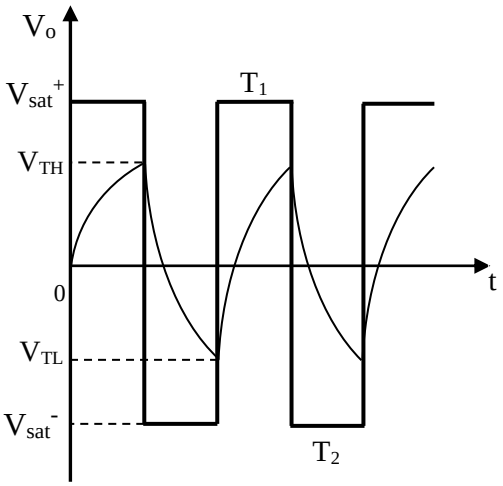


Fig. 4.9 Expected output waveform of the proposed square-wave generators

At this point of time, the current at the non-inverting terminal I_+ becomes less than the current at the inverting terminal I_- of the OTRA. Then the output changes its state from the upper saturation level V_{sat}^+ to the lower saturation level V_{sat}^- and the capacitor voltage V_C will start discharging to the lower threshold value V_{TL} instead of V_{sat}^-. Hence, the output voltage V_o changes its state from the on-duty cycle or higher saturation level V_{sat}^+ to off-duty cycle or lower saturation level V_{sat}^- when the non-inverting terminal current is equal to the inverting terminal current $I_+ = I_-$.

4.5 SUMMARY

In this chapter, the designs of new OTRA based waveform generators are presented. A generalized configuration to realize sinusoidal oscillators is presented with a single OTRA. Several possible realizations of sinusoidal oscillator circuits from the generalized configuration are discussed. All the presented sinusoidal oscillator circuits entail single OTRA. Twelve sinusoidal oscillators are realized from the generalized configuration.

In these twelve oscillator circuits, seven oscillator circuits are realized with a grounded passive component. Two special case oscillator circuits are also presented in this chapter with grounded resistance and capacitance. Most of the oscillator circuits realized from the generalized configuration is able to control the condition of oscillation and frequency of oscillation independently. In addition to the above oscillator circuits, two quadrature sinusoidal oscillator circuits are presented in this chapter. The proposed quadrature sinusoidal oscillators have the advantage of controlling the condition of oscillation and frequency of oscillation independently. At the end, two square waveform generators along with a few passive components are presented. The working of square waveform generator circuits and the transaction between the positive saturation level and negative saturation level is discussed in detail. The mathematical analysis of the newly proposed circuits is given in the next chapter.

CHAPTER 5

MATHAMETAICAL ANALYSIS OF THE PROPOSED WAVEFORM GENERATORS

5.1 INTRODUCTION

In this chapter, the mathematical analysis of the proposed circuits in chapter 4 is given. All the proposed circuits are designed with one or two OTRAs along with few passive components to generate the oscillations. In present days, the VLSI technology is evolving into a high level of chip integration with low voltage and low power. In the design of analogue signal processing circuits or waveform generators, the maximum number of active components and passive components should be decreased to achieve the high level of chip integration with low voltage and low power. The proposed circuits are constructed with less number of active and passive components.

5.2 GROUNDED RESISTANCE/CAPACITANCE BASED SINUSOIDAL OSCILLATORS

The generalized configuration to realize oscillator circuits is proposed in chapter 4 and the same is shown in Fig. 5.1.

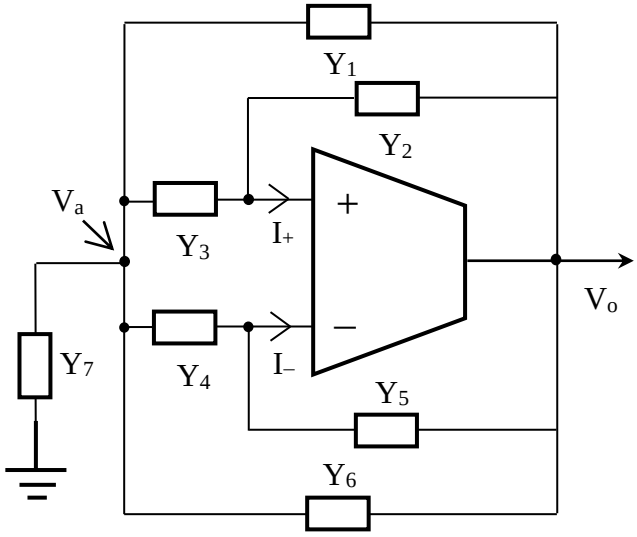


Fig. 5.1 Generalized configuration of the single OTRA based sinusoidal oscillators

The characteristic equation for the proposed generalized configuration shown in Fig. 5.1 can be derived from the ideal behavior of the OTRA. The currents at the

inverting and non-inverting terminals of the Fig. 5.1 can be written as in equations (5.1) and (5.2) are shown bellow.

$$V_0 Y_2 + V_a Y_3 = I_+ \tag{5.1}$$

$$V_0 Y_5 + V_a Y_4 = I_- \tag{5.2}$$

From the ideal terminal characteristics of the OTRA and from the equations (5.1) and (5.2), the voltage at the output terminal of the OTRA shown in Fig. 5.1 can be written as in (5.3).

$$V_0 = V_a \left(\frac{Y_4 - Y_3}{Y_2 - Y_5} \right) \tag{5.3}$$

Form the Fig. 5.1, the currents at the node V_a can be written as

$$V_0 (Y_1 + Y_6) = V_a (Y_1 + Y_3 + Y_4 + Y_6 + Y_7) \tag{5.4}$$

The generalized characteristic equation for the generalized oscillator circuit shown in Fig. 5.1 can be derived from the equations (5.3) and (5.4).

$$Y_1Y_2+Y_2Y_3+Y_2Y_4+Y_2Y_6+Y_2Y_7+Y_1Y_3+Y_3Y_6-Y_1Y_5-Y_1Y_4-Y_4Y_6-Y_3Y_5-Y_4Y_5-Y_5Y_6-Y_5Y_7=0 \tag{5.5}$$

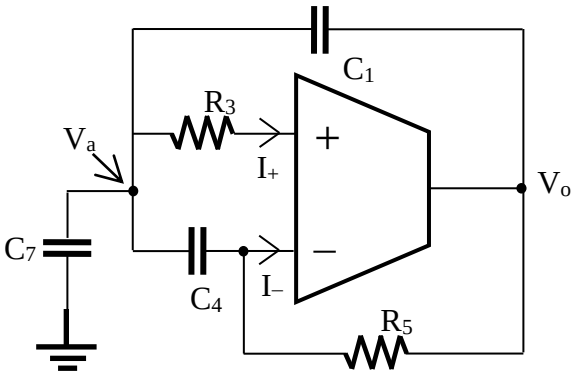


Fig. 5.2 OTRA based ooscillator circuit realized from Fig. 5.1

Where, Y_i*'s* are the admittances of the passive components. By proper selection of the passive components for the generalized configuration shown in Fig 5.1, many oscillator circuits can be generated. Some of the useful circuits generated from the generalized configuration are given in Fig. 4.3 and 4.4. The characteristic equations for the circuits shown in Fig. 4.3 and 4.4 can be derived by substituting admittances of the respective passive components. One of the proposed circuits in Fig. 4.4 is shown

in Fig. 5.2. The characteristic equation for the proposed circuit in Fig. 5.2 is derived from the generalized equation (5.5) by substituting the passive component $Y_1 = sC_1$, $Y_3 = R_3$, $Y_4 = sC_4$, $Y_5 = R_5$, $Y_7 = sC_7$ in place of Y_i's. The characteristic equation for the circuit in Fig. 5.2 can be written as

$$s^2(C_1C_4) + s(G_5(C_1 + C_4 + C_7) - C_1G_3) + G_5G_3 = 0 \qquad (5.6)$$

The condition of oscillation and frequency of oscillation for the circuit shown in Fig. 5.2 can be derived from the equation (5.6) as

Table 5.1. Condition of oscillations and frequency of oscillations for the proposed circuits in Fig. 4.3 and 4.4.

Oscillator circuits	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	C.O	F.O (ω_o^2)
Fig. 4.3	G_1	0	sC_2	G_3	sC_4	0	0	$C_4(R_1+R_3)=C_2R_3$	$\frac{1}{C_2C_4R_1R_3}$
Fig. 4.4 (a)	0	sC_2	G_3	sC_4	G_5	0	G_7	$C_2R_5(R_3+R_7) = C_4R_3R_7$	$\frac{(R_3+R_7)}{C_2C_4R_3R_5R_7}$
Fig. 4.4 (b)	sC_1	0	G_3	sC_4	G_5	0	sC_7	$R_3(C_1+C_4+C_7) = C_1R_5$	$\frac{1}{C_1C_4R_3R_5}$
Fig. 4.4 (c)	G_1	0	G_3	0	sC_5	sC_6	G_7	$C_6R_1R_7= C_5 (R_3R_7+ R_1R_7+R_1R_3)$	$\frac{1}{C_5C_6R_3R_1}$
Fig. 4.4 (d)	0	G_2	G_3	sC_4	G_5	sC_6	G_7	$R_3R_5(C_4+C_6)+ R_2R_5C_6=R_2R_3 (C_6+C_4)$	$\frac{(R_3+R_7)(R_2-R_5)}{R_2R_3R_5R_7C_4C_6}$
Fig. 4.4 (e)	0	G_2	sC_3	G_4	0	sC_6	G_7	$R_4(C_3+C_6) = C_6R_2$	$\frac{R_4+R_7}{R_2R_4R_7C_3C_6}$
Fig. 4.4 (f)	0	sC_2	G_3	sC_4	G_5	G_6	G_7	Equation (5.9)	Equation (5.10)
Fig. 4.4 (g)	0	sC_2	G_3	sC_4	0	G_6	G_7	$C_2(R_3+R_6+R_7)= C_4R_6\ R_3\ R_7$	$\frac{1}{C_2C_4R_3R_6}$
Fig. 4.4 (h)	sC_1	G_2	sC_3	G_4	G_5	0	0	$C_1R_4(R_2+R_5)=R_2 C_3 (R_4+R_5)$	$\frac{(R_2+R_5)-R_4}{R_2R_4R_5C_1C_3}$
Fig. 4.4 (i)	sC_1	sC_2	G_3	G_4	G_5	0	0	$C_1R_4(R_3+R_5)+ C_2R_3R_4=C_2R_3R_5$	$\frac{R_3+R_4+R_5}{C_1C_2R_3R_4R_5}$
C.O: Condition of oscillation, F.O: Frequency of oscillation, Y's are admittance of passive components									

Condition of oscillation (C.O): $R_3(C_1 + C_4 + C_7) = C_1R_5 \qquad (5.7)$

Frequency of Oscillation (F.O): $f = \frac{1}{2\pi}\sqrt{\frac{1}{C_1 C_4 R_5 R_3}}$ (5.8)

The condition of oscillation and frequency of oscillation for the circuit shown in Fig. 4.4(f) is given in equations (5.9) and (5.10).

$$R_5C_2\,(R_3R_6+R_6R_7+R_7R_3) = C_4R_7R_3\,(R_5+R_6) \tag{5.9}$$

$$f = \frac{1}{2\pi}\sqrt{\frac{R_3R_6 + R_7(R_3 + R_6 - R_5)}{C_2C_4R_3R_5R_6R_7}} \tag{5.10}$$

Similarly, the condition of oscillation and frequency of oscillation for all the proposed circuits in Fig. 4.3 and 4.4 can be derived from the generalized characteristic equation (5.7). The condition of oscillation and the frequency of oscillation for the proposed circuits in Fig. 4.3 and 4.4 are shown in Table.1. The characteristic equations to derive the condition of oscillation and frequency of oscillation for the circuits in Fig. 4.3 and 4.4 can also be derived individually without using the generalized characteristic equation. The currents at the non-inverting and inverting terminals of the OTRA based circuits shown in Fig. 5.2 is given in below equations.

$$I_+ = \frac{V_a}{R_3} \tag{5.11}$$

$$I_- = \frac{V_o}{R_5} + V_a sC_4 \tag{5.12}$$

From the ideal terminal characteristics of the OTRA, as stated in equation (2.1), the output terminal current of the OTRA shown in Fig. 5.2 is given in equation (5.13).

$$V_o = V_a R_5\left(\frac{1 - sC_4R_3}{R_3}\right) \tag{5.13}$$

The equation given in (5.14) is derived by writing Kirchhoff's Current Law (KCL) at the node V_a in Fig. 5.2.

$$V_o sC_1R_3 = V_a(1 + sR_3(C_4 + C_7 + C_1) \tag{5.14}$$

The characteristic equation for the circuit shown in Fig. 5.2 can be derived from the equations (5.13) and (5.14). The characteristic equation for the circuit in Fig. 5.2 is given in equation (5.15).

$$s^2 C_1 C_4 R_5 R_3 + s(R_3(C_1 + C_4 + C_7) - C_1 R_5) + 1 = 0 \qquad (5.15)$$

The condition of oscillation and frequency of oscillation derived from the equation (5.15) is given in equations (5.16) and (5.17).

$$\text{C.O} = R_3(C_1 + C_4 + C_7) = C_1 R_5 \qquad (5.16)$$

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{C_1 C_4 R_5 R_3}} \qquad (5.17)$$

The equations (5.7) and (5.8) for the condition of oscillation and frequency of oscillation is derived from the generalized characteristic equation and the equations (5.16) and (5.17) are the same. Likewise, the condition of oscillation and frequency of oscillation for all the proposed circuits in Fig. 4.2 and 4.3 can be derived by using generalized characteristic equation (5.5) or by applying general network laws to the respective circuits.

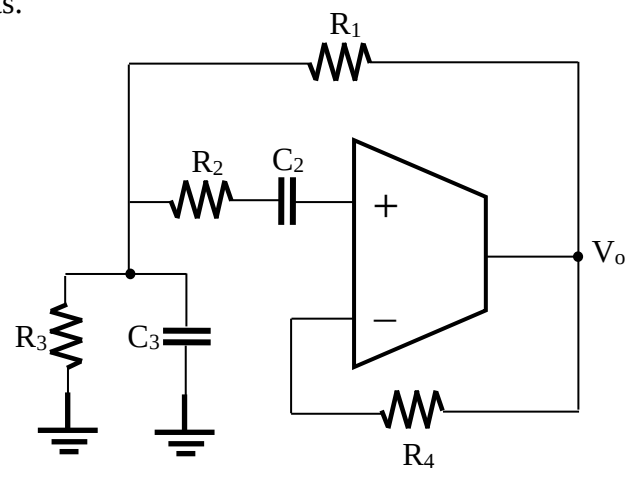


Fig. 5.3 Grounded resistance and capacitance sinusoidal oscillator circuit-I

The following passive components are chosen for the oscillator circuit shown in Fig. 5.3. $Y_1 = G_1$, $Y_2 = 0$, $Y_3 = sC_2G_2/(sC_2+G_2)$, $Y_4 = 0$, $Y_5 = G_4$, $Y_6 = 0$ and $Y_7 = G_3+sC_3$. The condition of oscillation and frequency of oscillation for the circuit shown in Fig. 5.3 are given in bellow equations.

$$C_2\left(\frac{R_2R_3+R_1R_3+R_2R_1}{R_1R_3R_4}\right)+\frac{C_3}{R_4}=\frac{C_2}{R_1} \tag{5.18}$$

$$f=\frac{1}{2\pi}\sqrt{\frac{R_1+R_3}{R_1R_2R_3C_2C_3}} \tag{5.19}$$

Similarly for the circuit shown in Fig. 5.4, the passive components are chosen as $Y_1= sC_1G_1/(sC_1+G_1)$, $Y_2 = 0$, $Y_3 = G_2$, $Y_4 = 0$, $Y_5 = G_4$, $Y_6 = 0$ and $Y_7 = G_3+sC_3$. The condition of oscillation and frequency of oscillation for the circuit shown in Fig. 5.4 is given in equations (5.20) and (5.21).

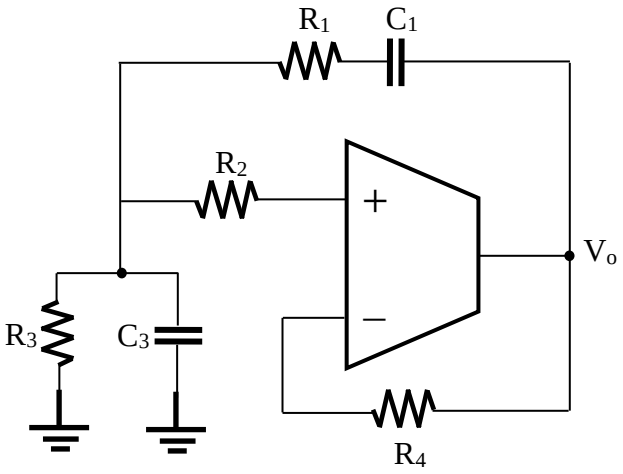


Fig. 5.4 Grounded resistance and capacitance sinusoidal oscillator circuit-II

$$C_1\left(\frac{R_2R_3+R_1R_3+R_2R_1}{R_2R_3R_4}\right)+\frac{C_3}{R_4}=\frac{C_1}{R_2} \tag{5.20}$$

$$f=\frac{1}{2\pi}\sqrt{\frac{R_2+R_3}{R_1R_2R_3C_1C_3}} \tag{5.21}$$

5.3 QUADRATURE SINUSOIDAL OSCILLATORS

The quadrature oscillator circuits proposed in Fig 4.6 and 4.7 are constructed by using two OTRAs and a few passive components to generate the sinusoidal oscillations with 90^o phase shift. The proposed quadrature sinusoidal oscillator circuits in chapter 4 are shown in Fig. 5.5 and 5.6 along with the current directions at the input and output terminals of the OTRAs are given for deriving the condition of

oscillation and frequency of oscillation. The inverting and non-inverting terminal currents of the OTRA-1 shown in Fig. 5.5 are given in equations (5.22) and (5.23).

$$I_{1+} = \frac{V_{01}}{R_1} \tag{5.22}$$

$$I_{1-} = V_{01} sC_2 + \frac{V_{02}}{R_5} \tag{5. 23}$$

From the ideal terminal characteristics of the OTRA stated in (2.1), the output terminal voltage V_{01} can be written as

$$V_{01} = V_{02}\left(\frac{R_1}{R_5(1 - sC_2R_1)}\right) \tag{5. 24}$$

Similarly, the current flowing into the inverting and non-inverting terminals of the OTRA-2 is given in equations (5.25) and (5.26).

$$I_{2+} = \frac{V_{01}}{R_3} \tag{5.25}$$

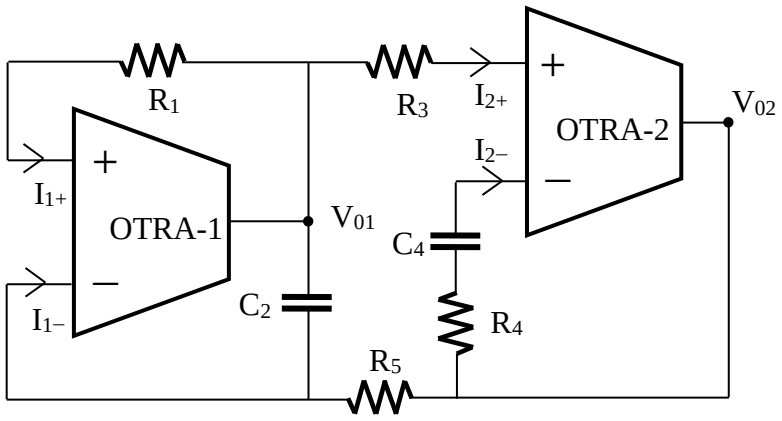


Fig. 5.5 Proposed quadrature sinusoidal oscillator circuit-I

$$I_{2-} = V_{02}\left(\frac{sC_4}{sC_4R_4 + 1}\right) \tag{5.26}$$

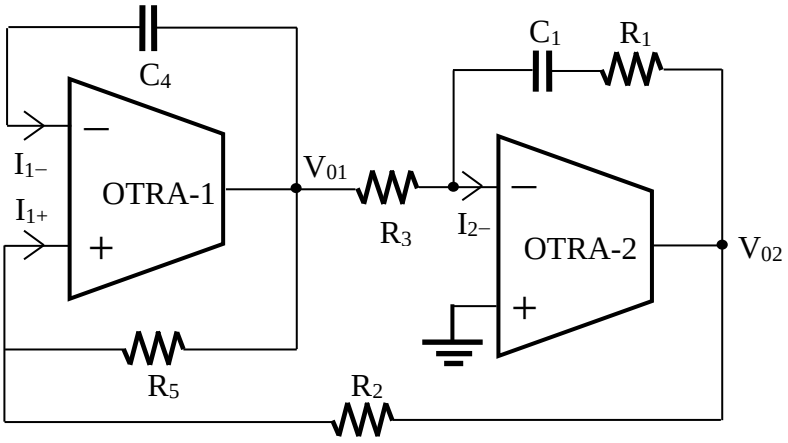


Fig. 5.6 Proposed quadrature sinusoidal oscillator circuit-II

The following equation can be written from the ideal terminal relations of the OTRA given in equation (2.1).

$$V_{01} = \frac{sC_4R_3}{sC_4R_4 + 1}V_{02} \tag{5.27}$$

The characteristic equation for the circuit shown in Fig. 5.5 can be derived from the equations (5.24) and (5.27) as

$$s^2\left(C_2C_4R_1R_3R_5\right) + sC_4\left(R_1R_4 - R_3R_5\right) + R_1 = 0 \tag{5.28}$$

From the above equation (5.28), the condition of oscillation and frequency of oscillation for the proposed quadrature sinusoidal oscillator circuit-I shown in Fig. 5.5 is given in equations (5.29) and (5.30).

$$\text{C.O:} \quad R_1R_4 = R_3R_5 \tag{5.29}$$

$$\text{F.O:} \quad f = \frac{1}{2\pi}\sqrt{\frac{1}{C_2C_4R_3R_5}} \tag{5.30}$$

From the equations (5.29) and (5.30), the frequency of oscillations can be controlled independently without affecting the condition of oscillation by using capacitor C_2 and C_4. Similarly, the condition of oscillation can be controlled independently without affecting the frequency of oscillation through the resistor R_1 and R_4.

The output voltage at the output terminal of the OTRA-1 shown in Fig. 5.6 can be derived by the ideal terminal behaviour of the OTRA. The output voltage V_{01} at the output terminal of the OTRA-1 is given in equation (5.31).

$$V_{01} = V_{02}\left(\frac{R_5}{sC_4R_5R_2 - R_2}\right) \tag{5.31}$$

Similarly, the output voltage V_{02} at the output terminal of the OTRA-2 shown in Fig. 5.6 is given in equation (5.32).

$$V_{02} = -V_{01}\left(\frac{sC_1R_1 + 1}{sC_1R_3}\right) \tag{5.32}$$

The characteristic equation for the quadrature sinusoidal oscillator circuit shown in Fig. 5.4 can be written from the equations (5.31) and (5.32).

$$s^2C_1C_4R_3R_2R_5 + sC_1\left(R_1R_5 - R_2R_3\right) + R_5 = 0 \tag{5.33}$$

The condition of oscillation and the frequency of oscillation for the circuit shown in Fig. 5.4 are given in equations (5.34) and (5.35).

$$\text{C.O:}\quad R_1R_5 = R_2R_3 \tag{5.34}$$

$$\text{F.O:}\quad f = \frac{1}{2\pi}\sqrt{\frac{1}{C_1C_4R_3R_2}} \tag{5.35}$$

From the equations (5.34) and (5.35), the frequency of oscillation can be controlled independently without affecting the condition of oscillation by using capacitor C_1 and C_4. Similarly, the condition of oscillation can be controlled independently without affecting the frequency of oscillation through the resistor R_1 and R_5.

5.4 SQUARE WAVEFORM GENERATORS

The proposed square waveform generator using single OTRA and three passive components is shown in Fig. 5.7. From the proposed square waveform generator shown in Fig. 5.7 and from the ideal behavior of the OTRA given in equation (2.1),

the voltage V_C of the capacitor C at the non-inverting terminal of the OTRA can be written as

$$\frac{V_C}{R_1} = \frac{V_o - V_C}{R_2} - \frac{V_C}{R_1} \tag{5.36}$$

The voltage V_C of the capacitor from the above equation is given in equation (5.37).

$$V_C = \left(\frac{R_1}{2R_2 + R_1} \right) V_o \tag{5.37}$$

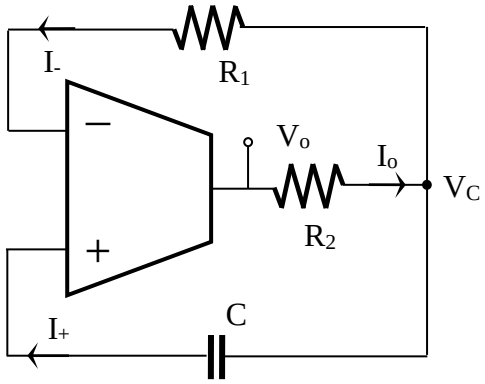


Fig. 5.7 Proposed square waveform generator using OTRA

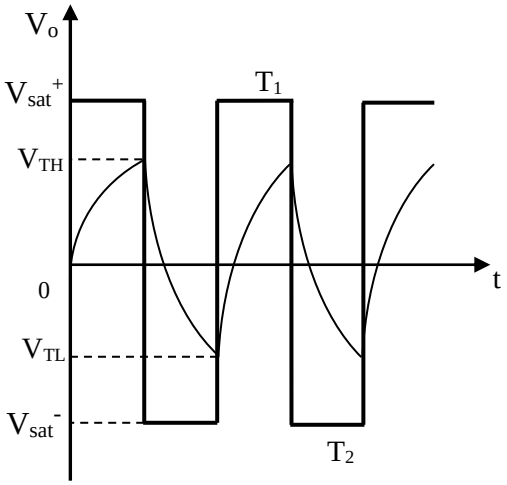


Fig. 5.8 Output waveform of the proposed circuit shown in Fig. 5.7

The output voltage V_o or the saturation levels V_{sat}^- and V_{sat}^+ changes its state when the non-inverting terminal current is equal to the inverting terminal current. Meanwhile

the capacitor voltage changes between V_{TH} and V_{TL}. Then the capacitor voltages can be derived from the equation (5.37).

$$V_{TH} = \left(\frac{R_1}{2R_2 + R_1} \right) V_{sat}^{+} \tag{5.38}$$

$$V_{TL} = \left(\frac{R_1}{2R_2 + R_1} \right) V_{sat}^{-} \tag{5.39}$$

The equation for the capacitor voltage $V_{C,}$ when it starts to increase from V_{TL} towards its final value V_{sat}^{+} can be expressed as.

$$V_c(t) = (V_{TL} - V_{sat}{}^{+}) e^{\frac{-T_1}{R_2 C}} + V_{sat}^{+} \tag{5.40}$$

The time period of the on-duty cycle T_1 can be derived from the equations (5.38), (5.39) and by making $V_C(t) = V_{TH}$ in equation (5.40).

$$T_1 = R_2 C \ln \left(\frac{\left(\frac{R_1}{2R_2 + R_1} \right) V_{sat}^{-} - V_{sat}^{+}}{\left(\frac{R_1}{2R_2 + R_1} \right) V_{sat}^{+} - V_{sat}^{+}} \right) \tag{5.41}$$

From the output square waveform shown in Fig. 5.8, it can be written $V_{sat}^{+} = -V_{sat}^{-}$.

$$\therefore \qquad T_1 = R_2 C \ln \left(1 + \frac{R_1}{R_2} \right) \tag{5.42}$$

The equation (5.42) is for the on-duty cycle (T_{ON}). At the end of on-duty cycle, the capacitor voltage V_C is charged up to the upper threshold voltage V_{TH}, instead of V_{sat}^{+}. At this point of time, the current at the non-inverting terminal I_+ becomes less than the current at the inverting terminal I_- of the OTRA. Then the output changes its state from the upper saturation level V_{sat}^{+} to the lower saturation level V_{sat}^{-} and the capacitor starts discharging. The voltage across capacitor C starts to decrease from higher threshold voltage $V_{TH,}$ it can be expressed as

$$V_c(t) = (V_{TL} - V_{sat}^-)e^{\frac{-T_2}{R_2C}} + V_{sat}^- \tag{5.43}$$

Time period T_2 can be derived by setting $V_C(t) = V_{TL}$ in the above equation.

$$T_2 = R_2C \ln\left(\frac{V_{TH} - V_{sat}^-}{V_{TL} - V_{sat}^-}\right) \tag{5.44}$$

By substituting the V_{TH} and V_{TL} values in the equation (5.44)

$$T_2 = R_2C \ln\left(1 + \frac{R_1}{R_2}\right) \tag{5.45}$$

The equation (5.45) is for the off-duty cycle (T_{OFF}). The final time period (T) of the waveform shown in the Fig. 5.8 is the sum of the on-duty cycle time period T_1 and off-duty cycle time period T_2 cycles.

$$T = T_{ON} + T_{OFF} = T_1 + T_2$$

$$T = 2R_2C \ln\left(1 + \frac{R_1}{R_2}\right) \tag{5.46}$$

From the above equation the frequency of the proposed circuit shown in Fig. 5.7 can be written as

$$f = \frac{1}{2R_2C \ln\left(1 + \frac{R_1}{R_2}\right)} \tag{5.47}$$

The second proposed square wave generator circuit shown in Fig. 5.9 is designed to vary both the duty cycles independently. Taking no cognizance of the voltage drop of the diodes, the frequency or time period equation for the proposed square-wave generator can be derived with the help of upper threshold V_{TH} and lower threshold V_{TL} voltages.

$$V_{TH} = \left(\frac{R_{12}}{2R_2 + R_{12}}\right)V_{sat}^+ \tag{5.48}$$

$$V_{TL} = \left(\frac{R_{11}}{2R_2 + R_{11}} \right) V_{sat}^{-} \tag{5.49}$$

From the capacitor voltage equation (5.40), the time period for the on-duty cycle can be expressed as

$$T_1 = R_2 C \ln \left(\frac{V_{TL} - V_{sat}^{+}}{V_{TH} - V_{sat}^{+}} \right) \tag{5.50}$$

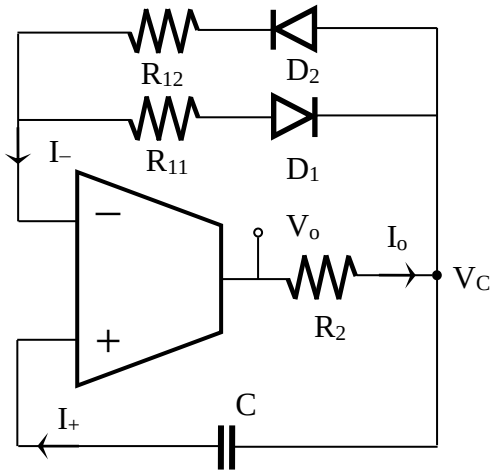


Fig. 5.9 Second proposed square-wave generator configuration

$$T_{ON} = R_2 C \ln \left(1 + \frac{R_{11}}{R_2} \right) \tag{5.51}$$

Similarly for the off-duty cycle time period, the T_{OFF} can be derived from the equation (5.37) by substituting the V_{TH} and V_{TL} from the equations (5.48) and (5.49).

$$T_{OFF} = R_2 C \ln \left(1 + \frac{R_{12}}{R_2} \right) \tag{5.52}$$

The total time period (T) for the proposed square-waveform generator shown in Fig. 5.9 can be expressed as

$$T = T_{ON} + T_{OFF}$$

$$T = R_2 C \ln \left(\left(1 + \frac{R_{11}}{R_2} \right) * \left(1 + \frac{R_{12}}{R_2} \right) \right) \tag{5.53}$$

The operating frequency of the proposed circuit shown in Fig. 5.9 can be calculated by substituting the passive component values in the below equation (5.48).

$$f = \frac{1}{R_2 C \ln\left(\left(1+\frac{R_{11}}{R_2}\right)*\left(1+\frac{R_{12}}{R_2}\right)\right)} \tag{5.54}$$

5.5 SUMMARY

This chapter is devoted to the mathematical analysis of the newly proposed circuits in chapter 4. All the proposed circuits are analyzed mathematically and the corresponding equations are discussed in detail. At first, the mathematical analysis of a generalized configuration is given. A generalized characteristic equation is derived from the generalized configuration. From this generalized characteristic equation, the condition of oscillation and the frequency of oscillation for all the proposed circuits are derived. The mathematical expressions of all the sinusoidal oscillator circuits are presented in a Table.

Most of the oscillator circuits realized from the generalized configuration is able to control the condition of oscillation and frequency of oscillation independently. Similarly, the same procedure is applied to derive the mathematical equations of two quadrature sinusoidal oscillators. In these quadrature sinusoidal oscillators, the condition of oscillation and frequency of oscillation can be controlled independently. Lastly, the mathematical expression for the time period of the proposed square waveform generator is given. The mathematical expressions of square waveform generator are derived by considering the charging and discharging voltages of the capacitor.

The mathematical analysis of all the proposed circuits is derived by considering the ideal terminal relation of the OTRA. The mathematical analysis based on the non-ideal model of OTRA is given in the next chapter.

CHAPTER 6

NON-IDEAL ANALYSIS OF THE PROPOSED CIRCUITS

6.1 INTRODUCTION

In previous chapter, the mathematical analysis is considered for the ideal characteristics of the OTRA. However, the ideal behavior of the OTRA is deviated, when it is considered for the practical implementation of the OTRA applications. This chapter describes the non-ideal analysis of the proposed circuits in chapter 4.

6.2 NON-IDEAL MODEL OF THE OTRA

The equivalent circuit models of the ideal and non-ideal OTRA is shown in Figs. 6.1 and 6.2.

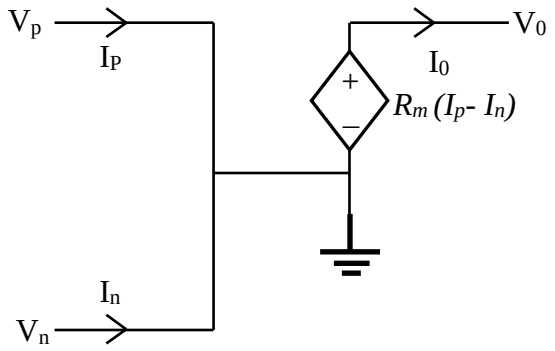


Fig. 6.1 Equivalent circuit model of the ideal OTRA

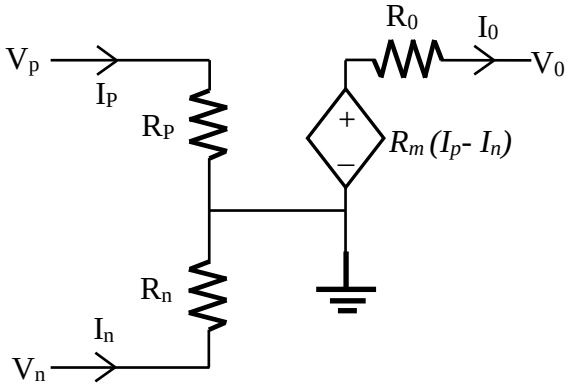


Fig. 6.2 Equivalent circuit model of the non-ideal OTRA

In OTRA, the output voltage is the difference of two input terminal currents multiplied by the transresistance gain R_m, which is ideally infinite. The inverting and non-inverting input terminals of the OTRA are internally grounded as shown in Fig. 6.1 and 6.2. The parasitic capacitances and resistances (R_p, R_n and R_0) associated with the input and output terminals of the OTRA are very small, grounded and negligible. Thus the most important non-ideality in OTRA is due to the finite transresistance gain R_m [42-44]. The finite transresistance gain R_m along with the frequency limitations associated with the OTRA must be considered in the analysis of the OTRA based circuits. Considering a single pole model for the transresistance gain R_m, then $R_m(s)$ can be expressed as

$$R_m = \frac{R_{mo}}{1 + \frac{j\omega}{\omega_o}} \tag{6.1}$$

Where R_{mo} is the DC open loop transresistance gain of the OTRA and ω_o is the pole angular frequency of the OTRA. For middle and high frequency applications, the transresistance gain R_m in s domain can be expressed as

$$R_m(s) = \frac{R_{mo}}{\frac{s}{\omega_o}} = \frac{1}{sC_p};\ C_p = \frac{1}{R_o \omega_o} \tag{6.2}$$

Where C_p is called the parasitic capacitance of the OTRA.

6.3 NON-IDEAL ANALYSIS OF THE GROUNDED RESISTANCE/CAPACITANCE BASED SINUSOIDAL OSCILLATORS

The generalized configuration proposed in chapter 4 is shown in Fig. 6.3 with the equivalent non-ideal OTRA model. The non-ideal analysis of the generalized configuration shown in Fig. 6.3 gives the following equations. The output voltage at the output terminal of the OTRA shown in Fig. 6.1 can be written as

$$V_0 = V_a \left(\frac{Y_4 - Y_3}{Y_2 - (Y_5 + Y_m)} \right) \tag{6.3}$$

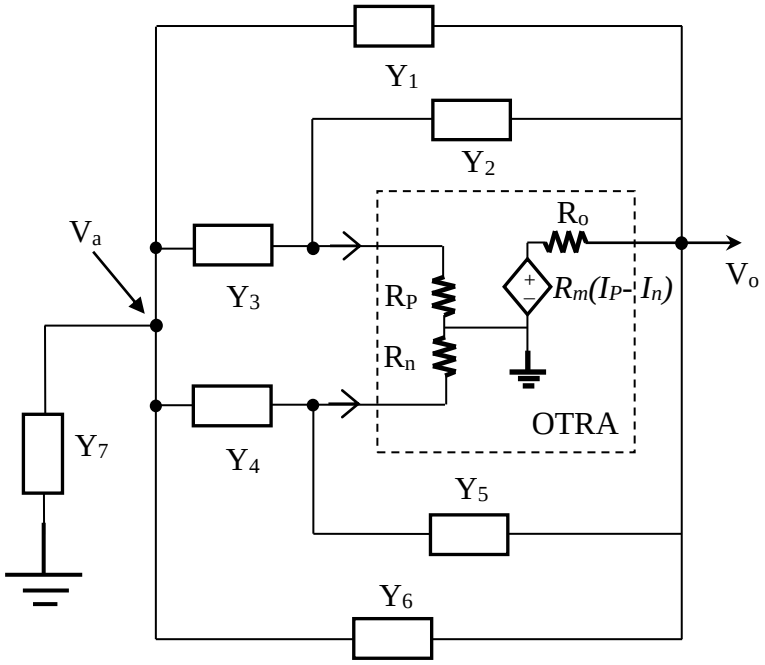


Fig. 6.3 Generalized configuration of the proposed oscillators in chapter 4

The following equation is derived by applying KCL at node 'a' shown in Fig. 6.3.

$$V_0(Y_1+Y_6)=V_a(Y_1+Y_3+Y_4+Y_6+Y_7) \tag{6.4}$$

The non-ideal equation for the generalized configuration shown in Fig. 6.3 is derived by substituting the equation (6.4) in (6.2).

$$Y_1Y_2+Y_2Y_3+Y_2Y_4+Y_2Y_6+Y_2Y_7+Y_1Y_3+Y_3Y_6-Y_1Y_5-Y_1Y_4-Y_4Y_6-Y_3Y_5-Y_4Y_5-Y_5Y_6-Y_5Y_7-$$

$$Y_m(Y_1+Y_3+Y_4+Y_6+Y_7)=0 \tag{6.5}$$

In the above equation, Y_i's are the admittances of the passive components and Y_m is the admittance of the transresistance gain. From the generalized non-ideal characteristic equation (6.5), the non-ideal equations for the proposed circuits in chapter 4 can be derived by substituting the passive components. The non-ideal condition of oscillation and frequency of oscillation for the proposed circuits in chapter 4 is given in Table 6.3. The condition of oscillation and frequency of oscillation for the proposed circuits can be derived independently without using the generalized characteristic equation as given in chapter 4. Likewise, the non-ideal

equations for the condition of oscillation and frequency of oscillation can also derive independently for the proposed circuits in chapter 4.

Table 6.1. Non-ideal condition of oscillations and frequency of oscillations for the proposed circuits in chapter 4.

Proposed designs	Condition of oscillation	Frequency of oscillation (ω_o^2)
Fig. 4.4 (a)	$R_5(C_2-C_P)(R_3+R_7) = C_4R_3R_7$	$\frac{R_3+R_7}{R_3R_5R_7C_4(C_2+C_P)}$
Fig. 4.4 (b)	$R_3(C_1+C_4+C_7)+C_PR_5=C_1R_5$	$R_3R_5(C_1C_4+C_P(C_1+C_4+C_7))$
Fig. 4.4 (c)	$C_6R_1R_7= (C_5+C_P)(R_3R_7+ R_1R_7+R_1R_3)$	$\frac{1}{R_1R_3(C_5+C_P)C_6}$
Fig. 4.4 (d)	$R_3R_5R_7(C_4+C_6)+ R_2R_7R_5(C_6-C_P)- R_2R_3R_5C_P = R_2R_3R_7(C_6+C_4)$	$\frac{(R_3+R_7)(R_2-R_5)}{R_2R_3R_5R_7(C_4C_6+C_P(C_4+C_6))}$
Fig. 4.4 (e)	$R_4R_7(C_3+C_6) = R_2R_7(C_6+C_P)+C_PR_4$	$\frac{R_4+R_7}{R_2R_4R_7(C_3C_6-C_P(C_3+C_6))}$
Fig. 4.4 (f)	Equation (6.6)	Equation (6.7)
Fig. 4.4 (g)	$(C_2+C_p)(R_3+R_6+R_7)=C_4R_6R_3R_7$	$\frac{1}{(C_2+C_p)C_4R_3R_6}$
Fig. 4.5 (a)	Equation (6.8)	Equation (6.9)
Fig. 4.5 (b)	Equation (6.10)	Equation (6.11)

The non-ideal condition of oscillation and frequency of oscillation for the circuit shown in Fig. 4.4 (f) is given in equations (6.6) and (6.7).

$$R_5C_2(R_3R_6+R_6R_7+R_7R_3) = C_4R_7R_3(R_5+R_6)+C_PR_5(R_3R_7+R_6R_7+R_3R_6) \quad (6.6)$$

$$f = \frac{1}{2\pi}\sqrt{\frac{R_3R_6+R_7(R_3+R_6-R_5)}{C_4(C_2-C_P)R_3R_5R_6R_7}} \quad (6.7)$$

The non-ideal condition of oscillation and frequency of oscillation for the circuit shown in Fig. 4.5 (a) is given in below equations.

$$C_2\left(\frac{R_2R_3+R_1R_3+R_2R_1}{R_1R_3R_4}\right)+\frac{C_3}{R_4}+C_P\left(\frac{R_1+R_3}{R_1R_3}\right)=\frac{C_2}{R_1} \tag{6.8}$$

$$f=\frac{1}{2\pi}\sqrt{\frac{R_1+R_3}{R_1R_2R_3\left(C_2C_3+C_PC_2\left(R_1R_2R_3+R_1R_2R_4+R_1R_3R_4+R_2R_3R_4\right)\right)}} \tag{6.9}$$

Similarly, for the proposed circuit shown in Fig. 4.5 (b), the non-ideal equations for the condition of oscillation and frequency of oscillation are given in equations (6.10) and (6.11).

$$C_1\left(\frac{R_2R_3+R_1R_3+R_2R_1}{R_2R_3R_4}\right)+\frac{C_3}{R_4}+C_P\left(\frac{R_2+R_3}{R_2R_3}\right)=\frac{C_1}{R_2} \tag{6.10}$$

$$f=\frac{1}{2\pi}\sqrt{\frac{R_2+R_3}{R_1R_2R_3\left(C_1C_3+C_PC_1\left(R_1R_2R_3+R_1R_2R_4+R_1R_3R_4+R_2R_3R_4\right)\right)}} \tag{6.11}$$

The non-ideal equations for the proposed circuits shown in Fig. 4.3, 4.4 and 4.5 can also be derived without using the generalized characteristic equation given in equation (6.5). For example, the non-ideal analysis of the circuit generated from the generalized configuration is shown in Fig. 6.2 is given bellow.

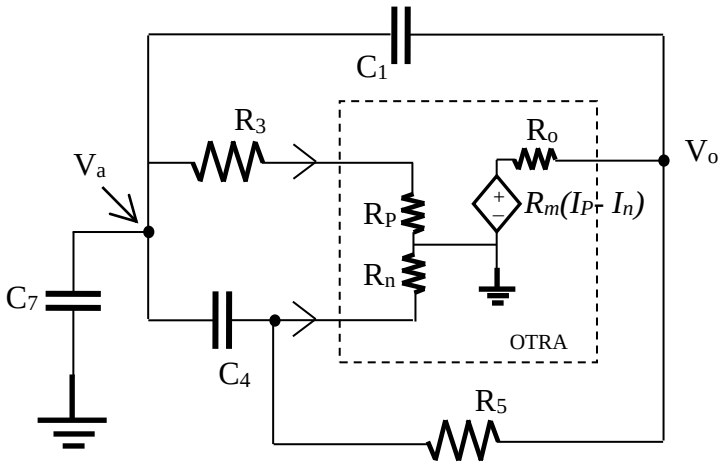


Fig. 6.4 Non-ideal OTRA based oscillator circuit

The currents at the inverting and non-inverting terminal of the OTRA shown in Fig. 6.4 can be written as

$$I_{+} = \frac{V_a}{R_3} \tag{6.12}$$

$$I_{-} = \frac{V_o}{R_5} + V_a sC_4 \tag{6.13}$$

From the terminal realtion of the OTRA, the following equation can be written as

$$V_o sC_P = V_a R_5 \left(\frac{1 - sC_4 R_3}{R_3} \right) \tag{6.14}$$

By applying Kirchhoff's Current Law (KCL) at the node V_a in Fig. 6.4

$$V_o sC_1 R_3 = V_a (1 + sR_3 (C_4 + C_7 + C_1) \tag{6.15}$$

From the equations (6.14) and (6.15), the non-ideal characteristic for the circuit shown in Fig. 6.2 can be written as

$$s^2 \left(R_3 R_5 \left(C_1 C_4 + C_P \left(C_1 + C_4 + C_7 \right) \right) \right) + s \left(R_3 \left(C_1 + C_4 + C_7 \right) + C_P R_5 - C_1 R_5 \right) + 1 = 0 \tag{6.16}$$

The non-ideal condition of oscillation and frequency of oscillation can be derived from the above equation.

$$R_3 \left(C_1 + C_4 + C_7 \right) + C_P R_5 = C_1 R_5 \tag{6.17}$$

$$f = \frac{1}{2\pi} \sqrt{\frac{1}{R_3 R_5 \left(C_1 C_4 + C_P \left(C_1 + C_4 + C_7 \right) \right)}} \tag{6.18}$$

6.4 NON-IDEAL ANALYSIS OF THE PROPOSED QUADRATURE SINUSOIDAL OSCILLATORS

The proposed quadrature sinusoidal oscillator in chapter 4 is shown in Fig. 6.5. From the Fig. 6.5 and from the non-ideal characteristics of the OTRA stated in equations (6.1) and (6.2), the output terminal voltage V_{01} can be written as

$$V_{01} = V_{02}\left(\frac{R_1 R_{m1}}{R_5\left(R_{m1} - R_1 - sC_2 R_1 R_{m1}\right)}\right) \tag{6.19}$$

Similarly, the output voltage V_{02} at the output terminal of the OTRA 2 is given in equation (6.20).

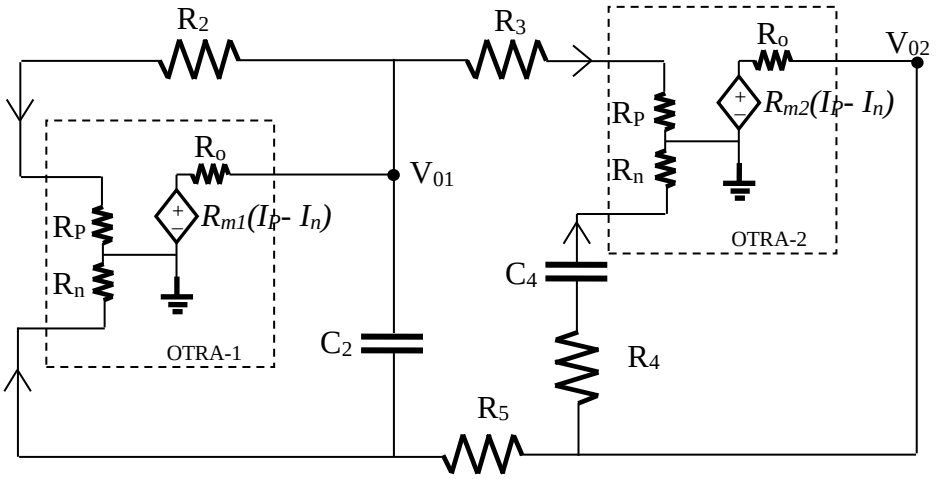


Fig. 6.5 Non-ideal model of the quadrature sinusoidal oscillator circuit proposed in chapter 4, Fig. 4.6

$$V_{01} = \frac{\left(sC_4R_4 + 1 + sC_4R_{m2}\right)R_3}{\left(sC_4R_4 + 1\right)R_{m2}} V_{02} \tag{6.20}$$

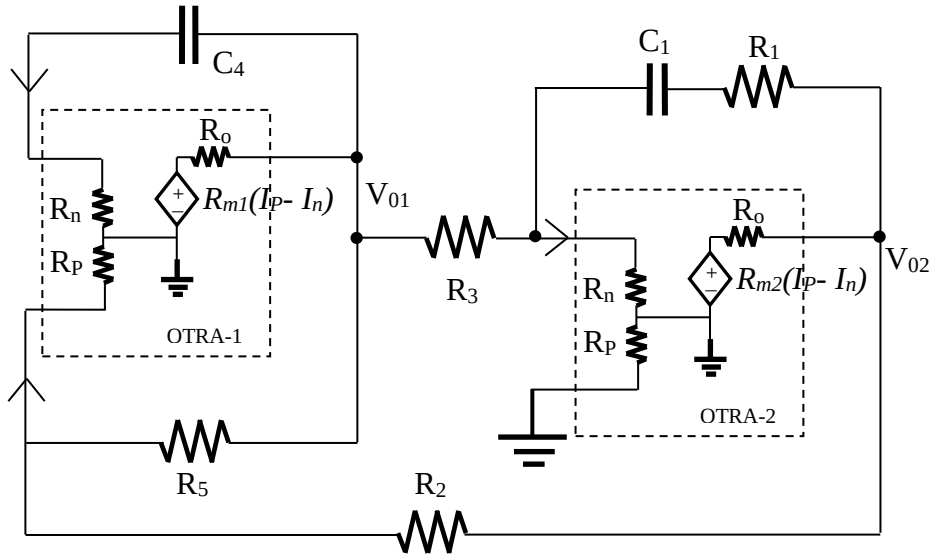


Fig. 6.6 Non-ideal model of the quadrature sinusoidal oscillator circuit proposed in chapter 4, Fig. 4.7

The non-ideal condition of oscillation and frequency of oscillation of the proposed circuit in Fig. 6.5 is given in equations (6.21) and (6.22).

$$\text{C.O:} \quad R_1 R_4 C_4 = R_3 R_5 \left(C_{p2} + C_4\right) \tag{6.21}$$

$$\text{F.O:} \quad f = \sqrt{\frac{R_1}{C_{p2} C_4 R_3 R_4 R_5 - R_1 R_3 R_5 \left(C_{p1} C_{p2} - C_{p2} C_2 - C_{p1} C_4 - C_2 C_4\right)}} \tag{6.22}$$

C_{p1} and C_{p2} are the parasitic capacitances associated with the OTRA 1 and OTRA 2 respectively.

Similarly, the condition of oscillation and frequency of oscillation for the proposed quadrature sinusoidal oscillator circuit shown in Fig. 6.6 is given in equation (6.23) and (6.24).

$$\text{C.O:} \quad R_1 R_5 C_1 = R_3 R_2 \left(C_{p2} + C_1\right) \tag{6.23}$$

$$\text{F.O:} \quad f = \sqrt{\frac{R_5}{R_2 R_3 \left(R_5 \left(C_1 C_4 + C_1 C_{p1} + C_4 C_{p2} + C_{p1} C_{p2}\right) - C_1 C_{p1} R_1\right)}} \tag{6.24}$$

C_{p1} and C_{p2} are the parasitic capacitances of the OTRA 1 and OTRA 2. It can be easily verified that, the condition of oscillation and frequency of oscillation equations (5.23), (5.24), (5.28) and (5.29) are given in chapter 5 from the ideal characteristics of OTRA can be derived by substituting $C_{p1} = C_{p2} = 0$ in the equations (6.21) - (6.24).

6.5 NON-IDEAL ANALYSIS OF THE PROPOSED SQUARE WAVEFORM GENERATORS

To consider the non-ideal and parasitic effects of the proposed circuits shown in Figs. 4.8 (a) and (b), an equivalent circuit model of the OTRA built with two current feedback amplifiers (CFAs) is shown in Fig. 6.7. A practical CFA (AD 844 AN IC) can be modeled as a positive second-generation current conveyor (CCII+) cascading a voltage buffer with finite parasitic resistances and non-zero current tracking errors.

Figure 6.7 reveals a more detailed circuit model of the OTRA, where R_x and R_z are the parasitic resistances and α represents the current tracking error factor from the terminal T_z with respect to the inverting input terminal. The standard values of R_x, R_z

and α are given in AD844AN datasheet are α = 0.98, R_x = 50 Ω, and R_z = 3 MΩ. The resulted expressions of the related currents are indicated in Fig. 6.7. The voltage tracking error effect between the CCII+ input terminals are skipped (eliminated) in the circuit model, because of the non-inverting terminal for each CCII+ are connected to ground. The non-ideal model of the proposed square wavefrom generator in chapter 4, Fig. 4.8 (a) is shown in Fig. 6.8. For the proposed circuit shown in Fig. 4.8 (a), the non-ideal analysis gives the following equations.

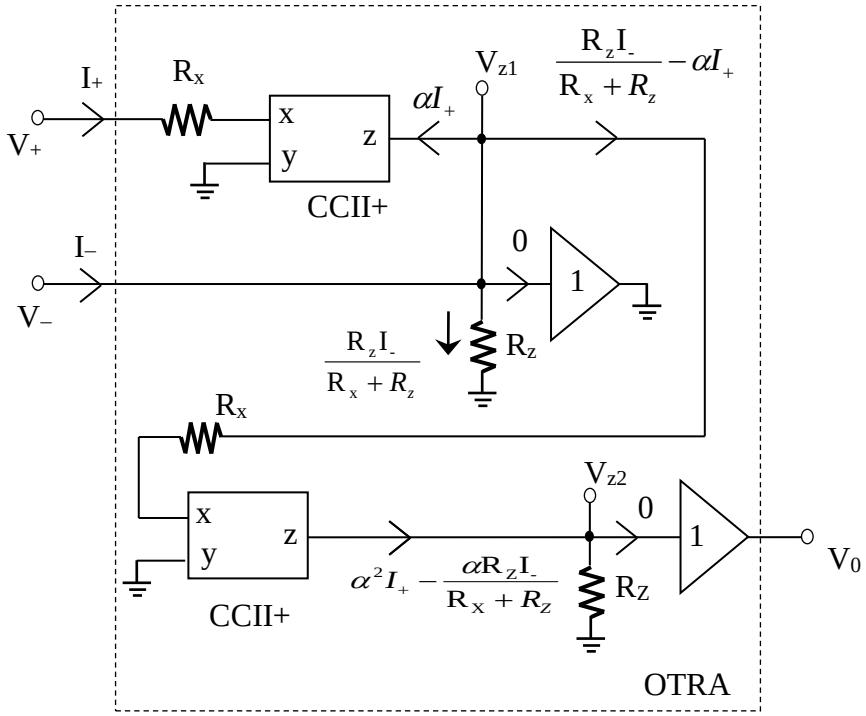


Fig. 6.7 Non-ideal model of the OTRA implemented with AD 844 ICs

$$V_{TH} = \left(\frac{\alpha R_1}{\alpha R_1 + R_2 \left(\frac{R_Z}{R_X + R_Z} + \alpha \right)} \right) V_{sat}^{+} \tag{6.25}$$

$$V_{TL} = \left(\frac{\alpha R_1}{\alpha R_1 + R_2 \left(\frac{R_Z}{R_X + R_Z} + \alpha \right)} \right) V_{sat}^{-} \tag{6.26}$$

The equations for the on-duty cycle and off-duty cycle can be expressed as

$$T_1 = R_2 C \ln\left(\frac{V_{TL} - V_{sat}^-}{V_{TH} - V_{sat}^-}\right) \tag{6.27}$$

$$T_2 = R_2 C \ln\left(\frac{V_{TH} - V_{sat}^-}{V_{TL} - V_{sat}^-}\right) \tag{6.28}$$

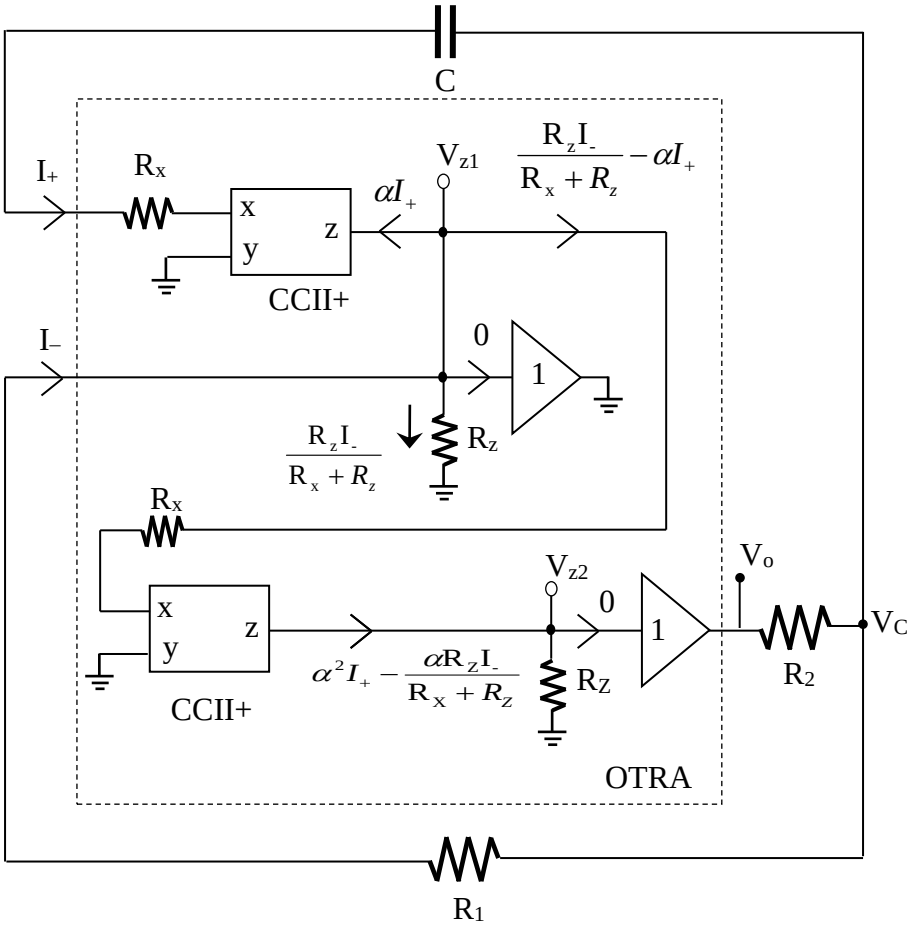


Fig. 6.8 Non-ideal model of the proposed square waveform generator

Substituting these higher and lower threshold voltage equations (6.25) & (6.26) in equation (6.27) and (6.28), the non-ideal time period for the proposed circuit in chapter 4, Fig. 4.8 (a) can be expressed as

$$T = 2R_2 C \ln\left(1 + \frac{2\alpha R_1}{R_2\left(\frac{R_Z}{R_X + R_Z} + \alpha\right)}\right) \tag{6.29}$$

The non-ideal equation for the second proposed circuit shown in Fig. 4.8 (b), chapter 4 is given in equation (6.30).

$$T = R_2 C \ln\left(\left(1+\frac{2\alpha R_{11}}{R_2\left(\frac{R_Z}{R_X+R_Z}+\alpha\right)}\right)*\left(1+\frac{2\alpha R_{12}}{R_2\left(\frac{R_Z}{R_X+R_Z}+\alpha\right)}\right)\right) \qquad (6.30)$$

It can be easily verified that, the equation (6.29) and (6.30) are reduced to equation (5.40) and (5.47) by substituting the ideal OTRA characteristics, when $\alpha \approx 1$ and $R_x \approx 0$.

6.6 SUMMARY

In this chapter, the non-ideal analysis of all the proposed circuits is given. All the proposed circuits are re-examined by considering the non-ideal model of the OTRA. The non-ideal condition of oscillation and frequency of oscillation for the sinusoidal oscillator circuits realized from the generalized configuration is presented in a Table. A generalized non-ideal characteristic equation is derived for the proposed sinusoidal oscillator circuits. From this non-ideal characteristic equation, the non-ideal condition of oscillation and non-ideal frequency of oscillation is derived. Similarly, the same procedure is followed to derive the non-ideal condition of oscillation and frequency of oscillation for the quadrature sinusoidal oscillators.

At last, the non-ideal time period equations are derived for the square waveform generators by considering the parasitic resistances and current tracking errors of practical model of OTRA.

CHAPTER 7

SIMULATION RESULTS

7.1 INTRODUCTION

In this chapter, the simulation results for the newly proposed circuits in chapter 4 using either single or two OTRA active elements are given. All the proposed circuits given in chapter 4 are designed using one or two OTRAs along with few passive components. All the proposed circuits are simulated for waveform generation by using the CMOS OTRA shown in Fig. 7.1. The CMOS OTRA shown in Fig. 7.1 is designed using Cadence 180 nm CMOS model parameters and simulated by using Spectre simulation model parameters. For simulation, the supply voltages ± 1.8 V are used for all the proposed circuits.

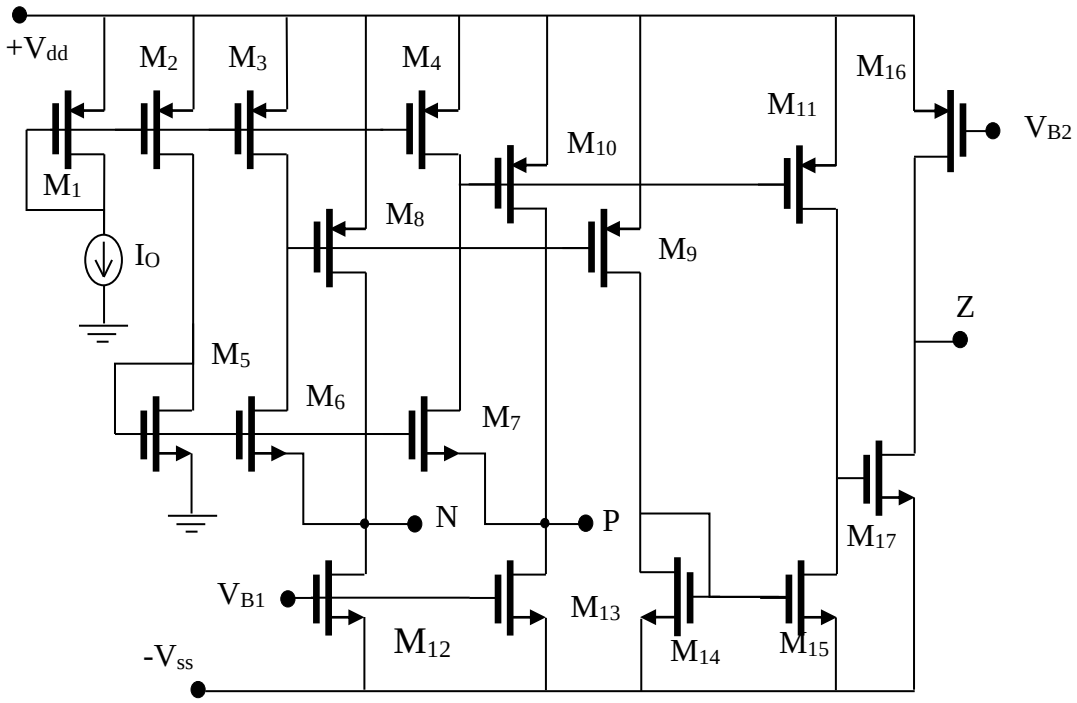


Fig. 7.1 CMOS implementation of the OTRA

The widths and lengths of transistors used for simulating the CMOS OTRA by Cadence gpdk 180nm are given in Table 7.1 and the bias current used during the simulation is I_o = 80µA.

Table 7.1 Aspect ratios of CMOS OTRA shown in Fig. 7.1

Transistor	Width (μm)	Length (nm)
M_1, M_2, M_3, M_4	2	180
M_5, M_6, M_7	2	180
M_8	4.5	180
M_9	9	180
M_{10}, M_{11}	40	180
M_{12}, M_{13}	40	180
M_{14}, M_{15}	33	180
M_{16}	22	180
M_{17}	12	180

7.2 GROUNDED RESISTANCE/CAPACITANCE SINUSOIDAL OSCILLATORS

7.2.1 SIMULATION RESULTS

The passive components for the newly proposed topologies shown in Fig. 4.3 and 4.4 are connected to the respective terminals of the CMOS OTRA shown in Fig. 7.1. All newly proposed circuits are simulated using Spectre simulation model parameters.

For the first proposed minimum component oscillator circuit shown in Fig. 4.3, the passive components R_1 = 10 kΩ, R_3 = 1 kΩ, C_2 = 100 pF and C_4 = 1 nF are connected for generating the oscillations. Fig. 7.2 represents the simulated output waveform of the first proposed minimum component oscillator circuit with a frequency of 161.5 kHz.

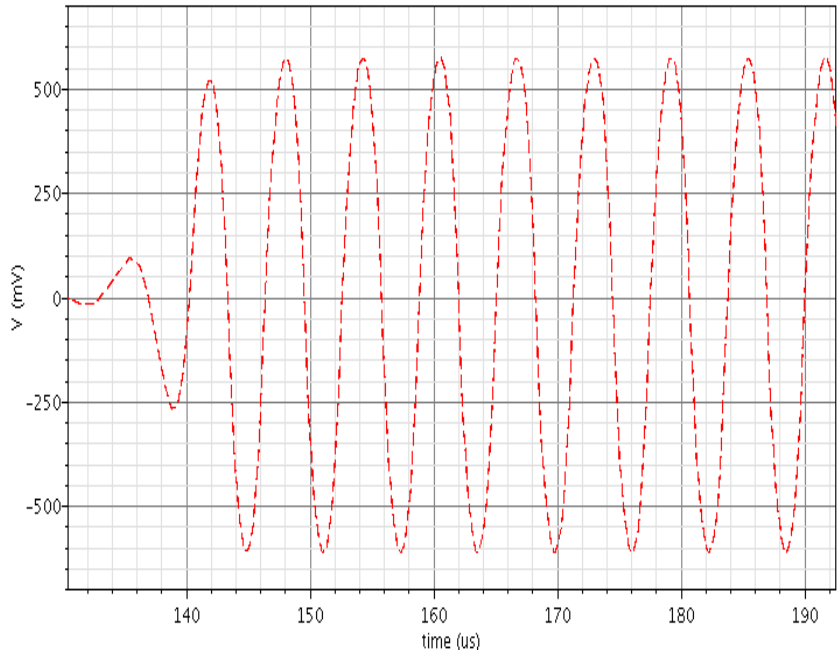


Fig. 7.2 Simulated output waveform of the proposed circuit in Fig. 4.3

The percentage of error between the simulated and theoretical oscillation frequency is 1.5 %. The frequency spectrum of the proposed circuit shown in Fig. 4.3 is shown in Fig. 7.3.

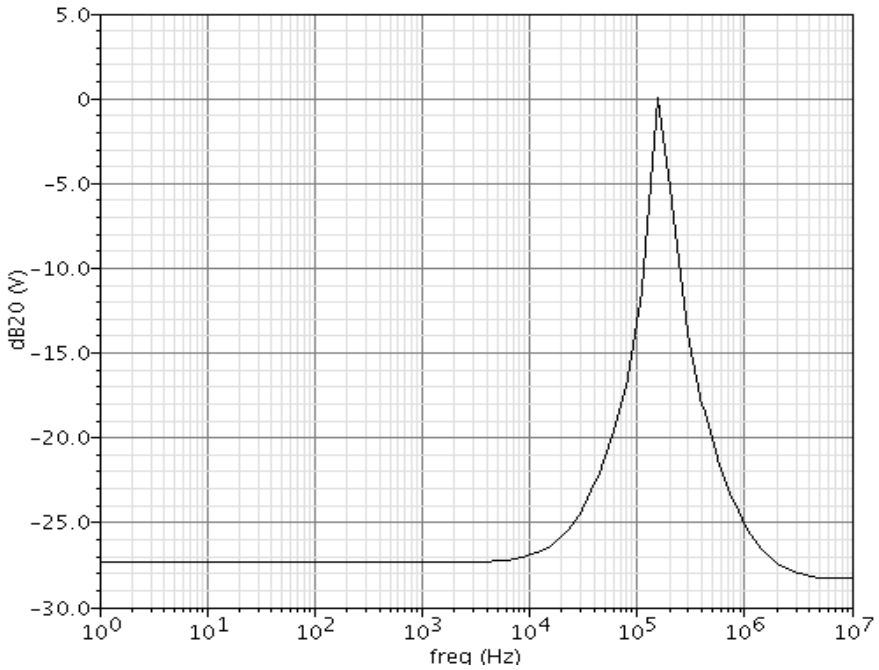


Fig. 7.3 Frequency spectrum of the proposed circuit in Fig. 4.3

The following passive components R_3 = 60 Ω, R_5 = 1 kΩ, R_7 = 300 Ω, C_2 = 10 nF and C_4 = 100 nF are used to simulate the proposed circuit shown in Fig. 4.4 (a). Figure 7.4 represent the output waveform of the proposed oscillator circuit with a frequency of 21.8 kHz. The percentage of error between the simulated and theoretical oscillation frequency is 2.8 %.

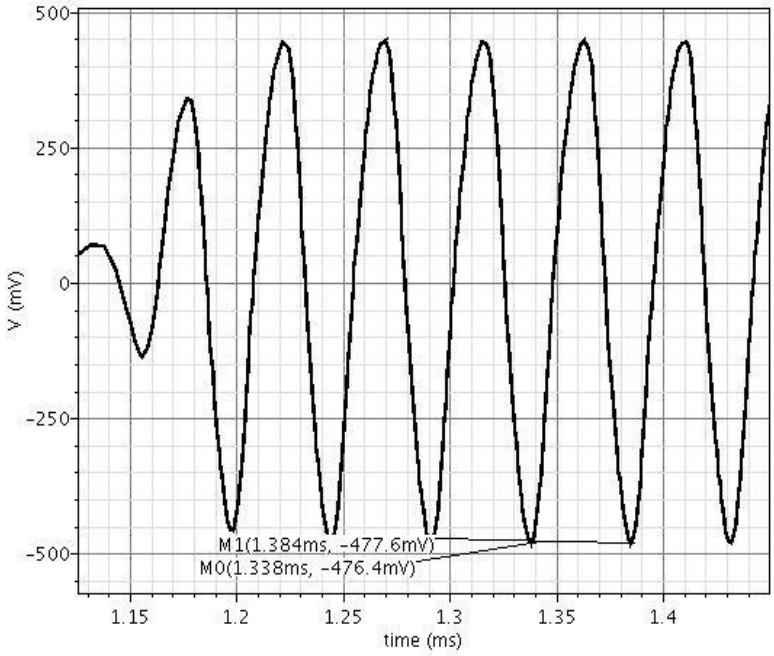


Fig. 7.4 Simulated output waveform of the proposed circuit in Fig. 4.4 (a)

The proposed circuit in Fig. 4.4 (b) is connected with the passive components C_1 = 100 pF, C_4 = 100 pF, C_7 = 100 pF, R_3 = 150 Ω, R_5 = 500 Ω for waveform generation. The simulated output waveform of the oscillator circuit shown in Fig. 4.4 (b) is shown in Fig. 7.5. The simulated oscillation frequency for the oscillator circuit shown in Fig. 4.4 (b) is 5.3 MHz which is close to the theoretically calculated frequency of 5.78 MHz. The following passive components are chosen for generating the oscillations in the proposed circuit shown in Fig. 4.4 (c), R_1 = 1 kΩ, R_3 = 150 Ω, R_7 = 15 Ω, C_5 = 10 pF and C_6 = 100 pF. The simulated output waveform for the proposed circuit shown in Fig. 4.4 (c) is shown in Fig. 7.6. The oscillation frequency of the waveform shown in Fig. 7.6 is at 12.9 MHz. The simulated output waveform of the proposed circuit shown in Fig. 4.4 (d) is presented in Fig. 7.7, which is obtained for the passive components R_2 = 500 Ω, R_3 = 12 kΩ, R_5 = 400 Ω, R_7 = 2 kΩ, C_4 = 100 pF and C_6 = 10 pF. The simulated oscillation frequency of the proposed circuit shown in Fig. 4.4 (d) is 2.9 MHz.

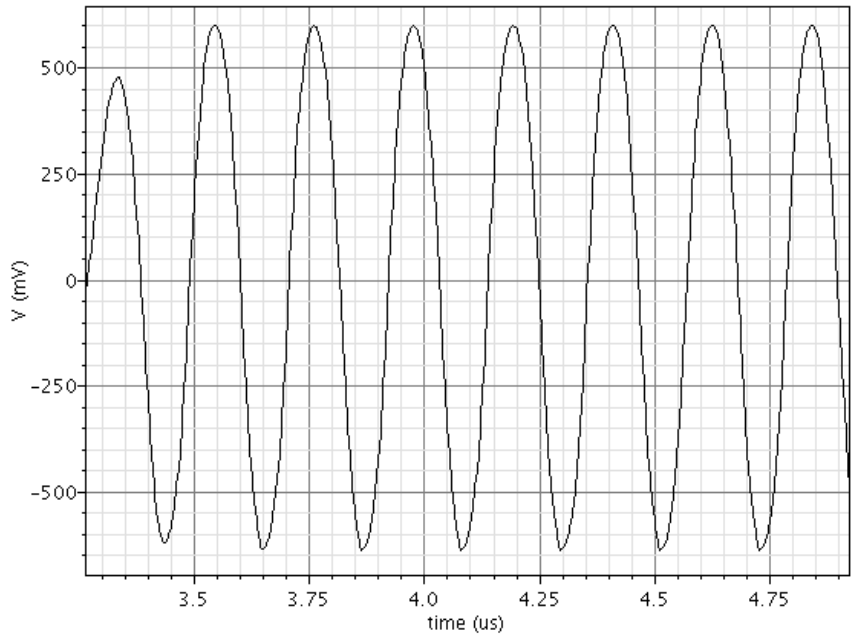


Fig. 7.5 Simulated output waveform of the proposed circuit in Fig. 4.4 (b)

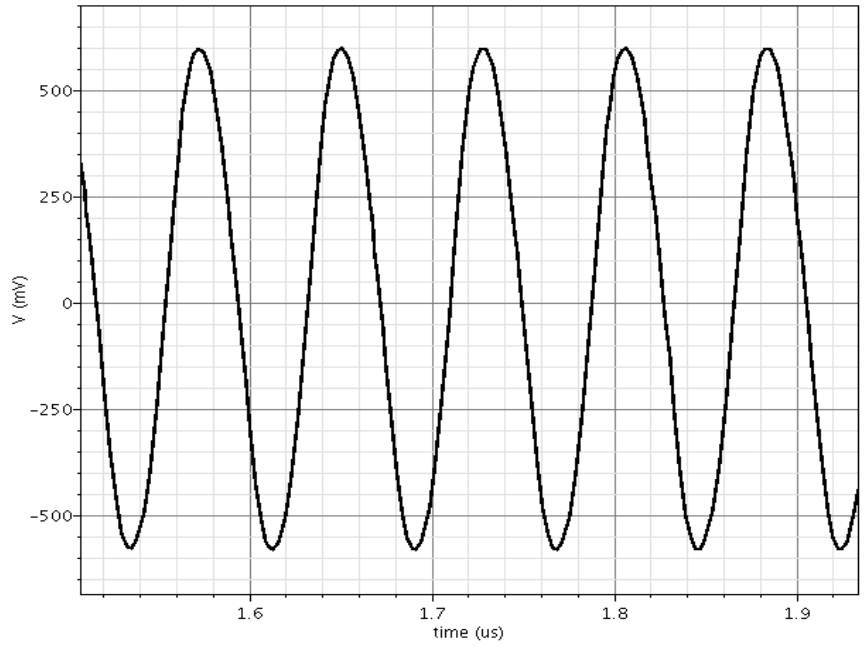


Fig. 7.6 Simulated output waveform of the proposed circuit in Fig. 4.4 (c)

The variation of oscillation frequency with respect to the passive component connected to the circuit is shown in Fig. 7.8 for the proposed circuit in Fig. 4.4 (d). For this figure, the passive components values chosen to be C_4 = 100 pF, C_6 = 10 pF, R_2 = 500 Ω, R_3 = 12 kΩ, R_5 = 400 Ω and R_7 is varied from 1 kΩ to 12 kΩ.

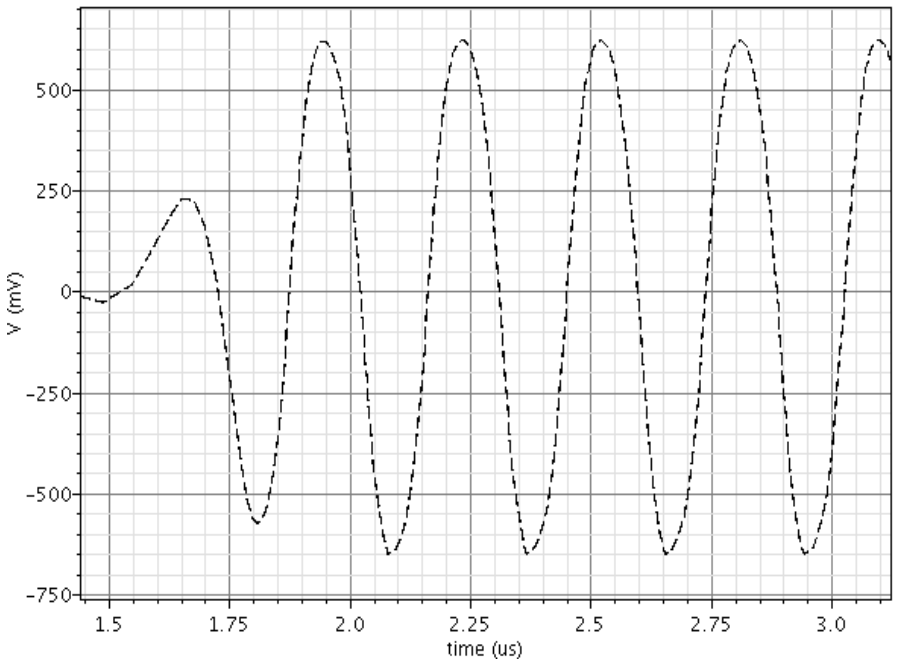


Fig. 7.7 Simulated output waveform of the proposed circuit in Fig. 4.4 (d)

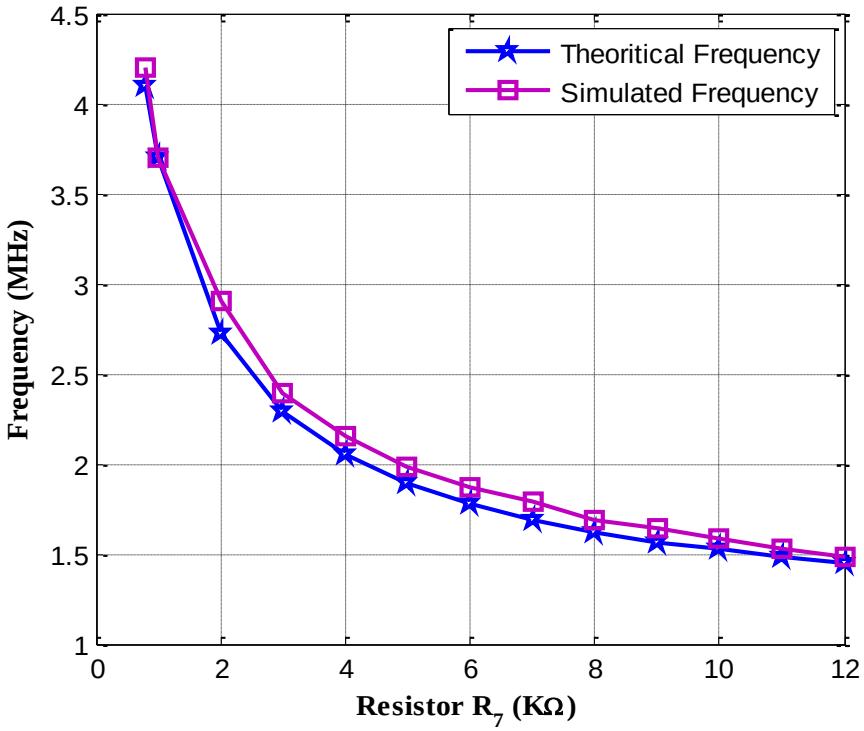


Fig. 7.8 Tunability of the proposed circuit in Fig. 4.4 (d) with respect to the resistor R_7

The passive components R_2 = 1 kΩ, R_4 = 60 Ω, R_7 = 50 Ω, C_6 = 100 pF and C_3 = 10 pF are used for producing the oscillations in the proposed circuit shown in Fig. 4.4 (e). The simulated output waveform of the proposed circuit is given in Fig. 7.9 with a frequency of 3.15 MHz, whereas the theoretical oscillation frequency was

calculated as 3.02 MHz. The variation of oscillation frequency for Fig. 4.4 (e) with respect to the passive component connected to the circuit is shown in Fig. 7.10. For this figure, the passive components values are C_3 = 10 pF, C_6 = 100 pF, R_2 = 1 kΩ, R_4 = 60 Ω chosen and R_7 is varied from 50 Ω to 10 kΩ.

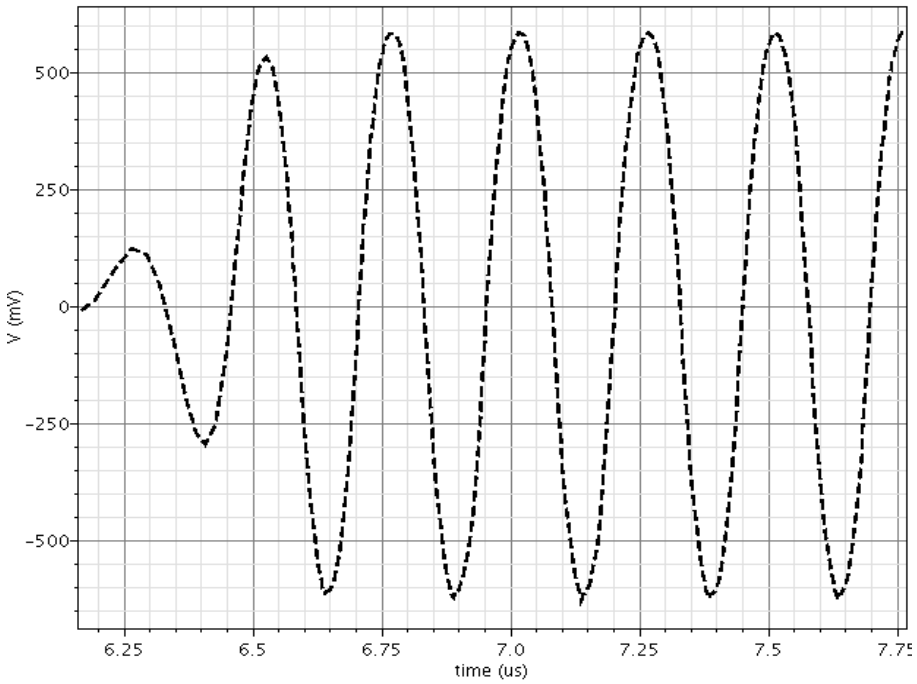


Fig. 7.9 Simulated output waveform of the proposed circuit in Fig. 4.4 (e)

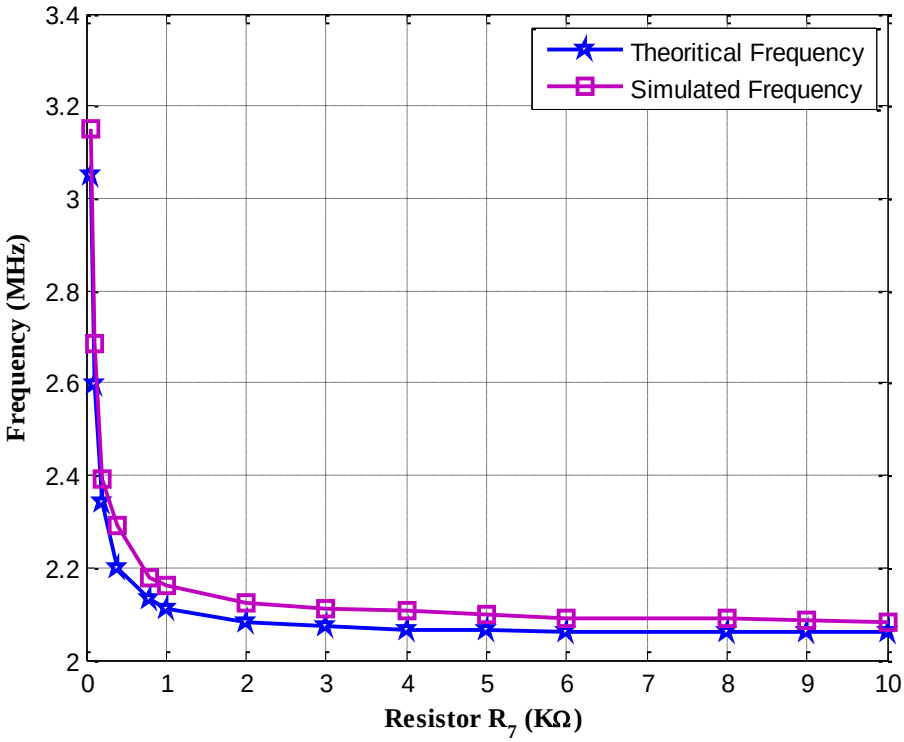


Fig. 7.10 Tunability of the proposed circuit in Fig. 4.4 (e) with respect to the resistor R_7

For generating the oscillations of the proposed circuit shown in Fig. 4.4 (f), the passive component values are chosen to be R_3 = 100 Ω, R_5 = 1 kΩ, R_6 = 7 kΩ, R_7 = 200 Ω, C_2 = 100 pF and C_4 = 10 pF. Fig. 7.11 represents the simulated output waveform of the proposed circuit with a frequency of 1.3 MHz which is close to the theoretical result of 1.8 MHz. For generating the oscillations of the proposed circuit shown in Fig. 4.4 (g), the passive component values are chosen to be R_3 = 1 kΩ, R_6 = 1 kΩ, R_7 = 5 kΩ C_1 = 100 pF and C_4 = 100 pF. Fig. 7.12 represents the simulated output waveform of the proposed circuit with a frequency of 1.2 MHz which is close to the theoretical result of 1.5 MHz.

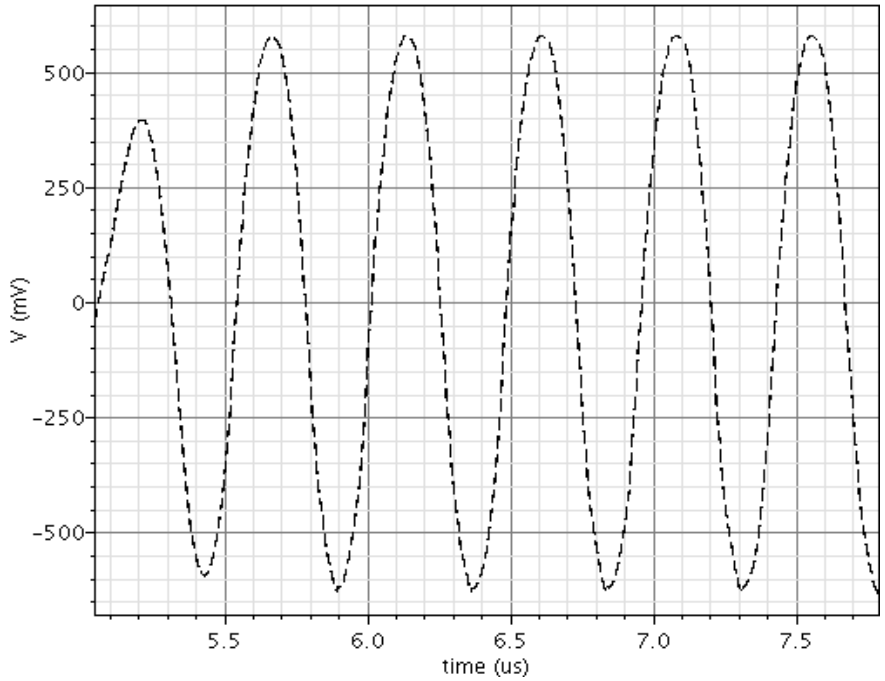


Fig. 7.11 Simulated output waveform of the proposed circuit in Fig. 4.4 (f)

The proposed circuit in Fig. 4.4(h) is constructed with passive components C_1 = 10 nF, C_3 = 100 nF, R_2 = 100 Ω, R_4 = 1 kΩ, and R_5 = 4 kΩ to generate the oscillations. The corresponding waveform at the output terminal of the proposed circuit is shown in Fig. 7.13. The simulated output waveform frequency for the proposed circuit is 14 kHz, which is very near to the theoretical value of 14.2 kHz.

The passive components values C_1 = 10 nF, C_2 = 100 nF, R_3 = 100 Ω, R_4 = 1 kΩ and R_5 = 5 kΩ are used to produce the oscillations in the proposed circuit shown in Fig. 4.4(i). The corresponding output waveform is shown in Fig. 7.14 at 16.5 kHz.

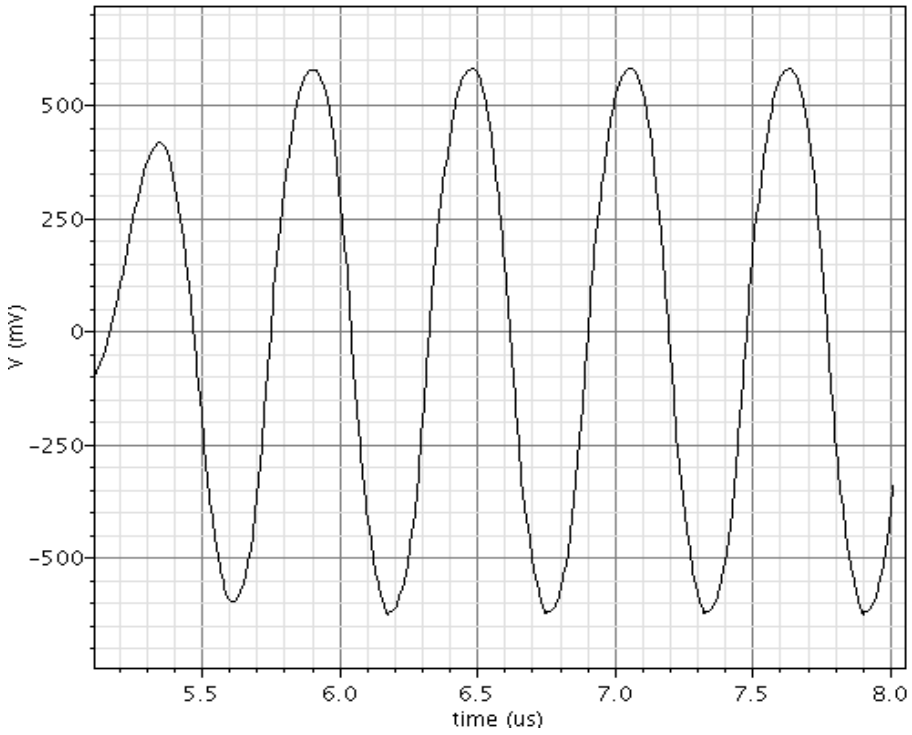


Fig. 7.12 Simulated output waveform of the proposed circuit in Fig. 4.4 (g)

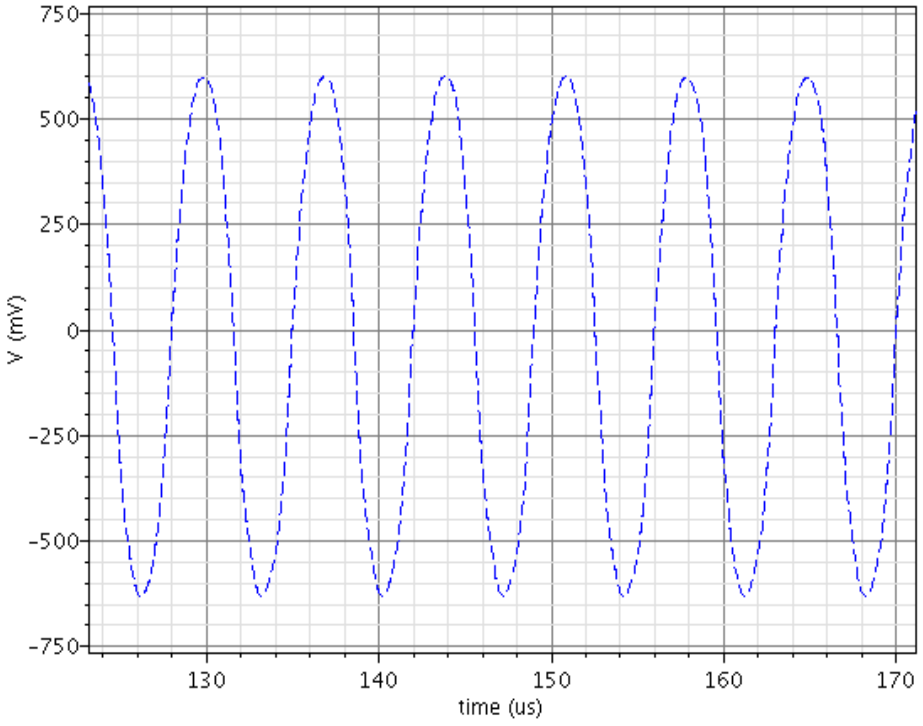


Fig. 7.13 Simulated output waveform of the proposed circuit in Fig. 4.4 (h)

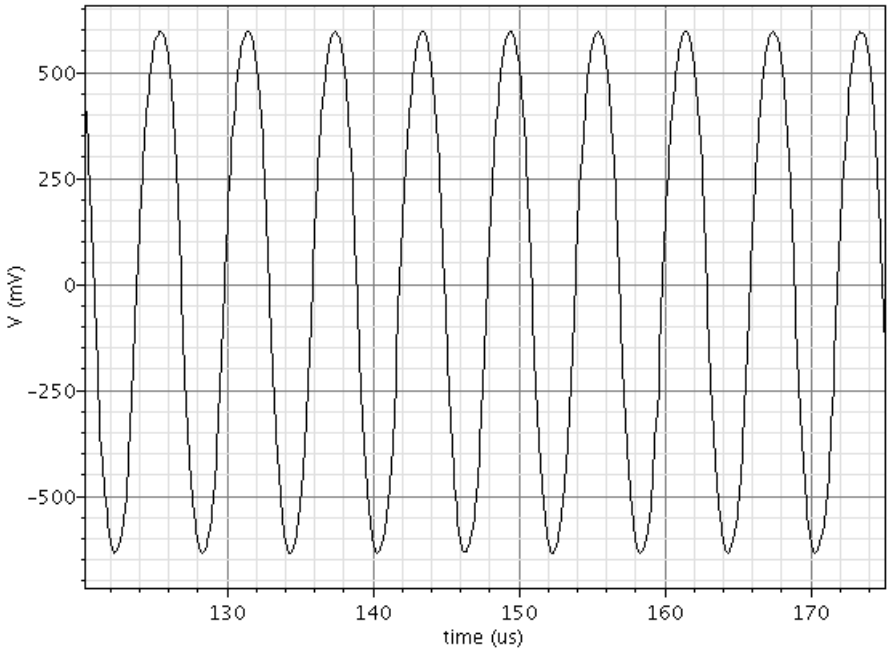


Fig. 7.14 Simulated output waveform of the proposed circuit in Fig. 4.4 (i)

The following passive component values are chosen to simulate the proposed circuit in Fig. 4.5 (a), R_1 = 100 Ω, R_2 = 1.2 kΩ, R_3 = 600 Ω, R_4 = 5.5 kΩ, C_2 = 100 pF and C_3 = 100 pF. Fig. 7.15 represents the simulated output waveform of the proposed circuit in Fig. 4.5 (a) with a frequency of 3.1 MHz.

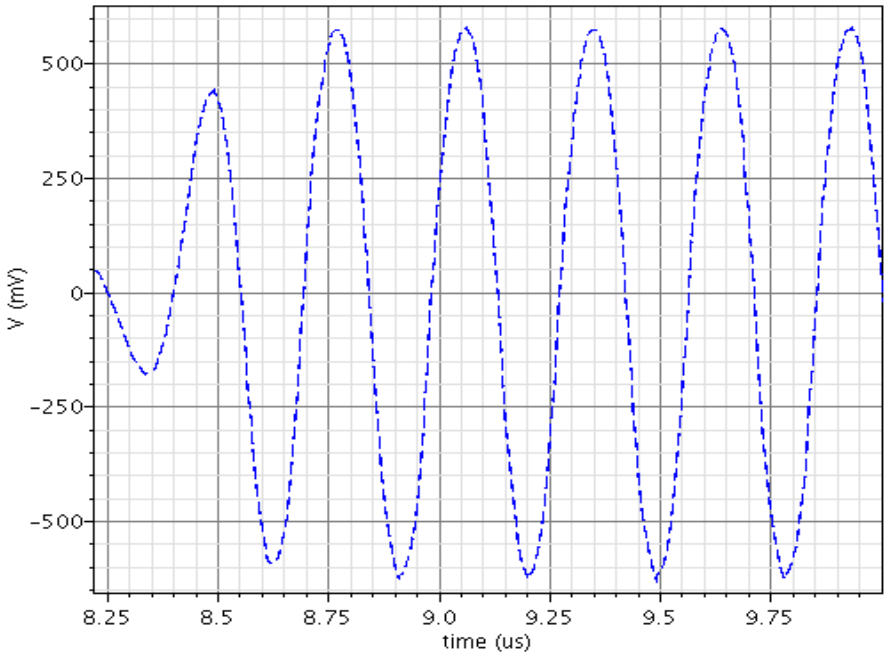


Fig. 7.15 Simulated output waveform of the proposed circuit in Fig. 4.5 (a)

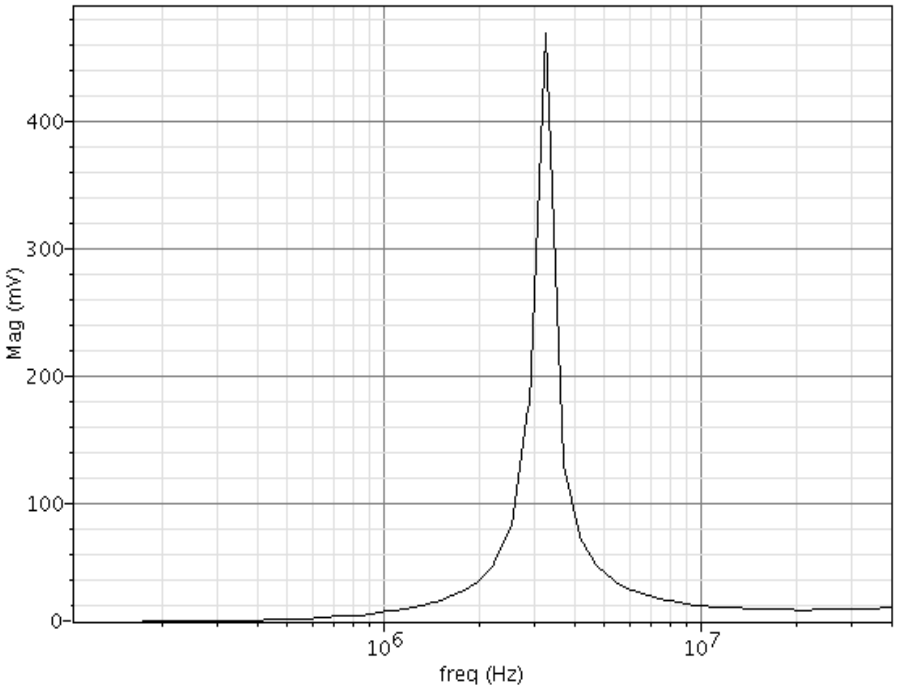


Fig. 7.16 Frequency spectrum of the proposed circuit in Fig. 4.5 (a)

The simulated frequency in Fig. 7.15 is very close to the theoretical frequency of 3.21 MHz. The frequency spectrum of the proposed circuit in Fig. 4.5 (a) is shown in Fig. 7.16.

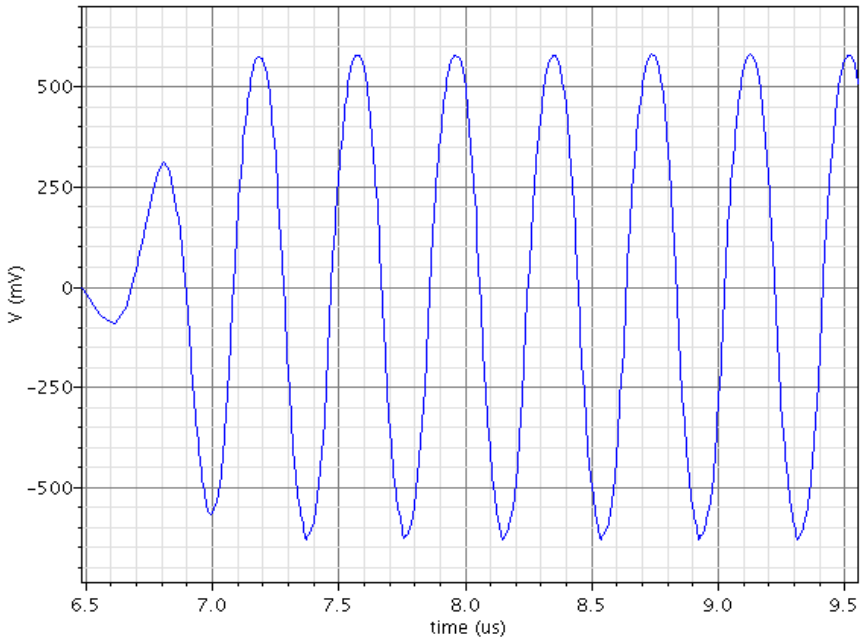


Fig. 7.17 Simulated output waveform of the proposed circuit in Fig. 4.5 (b)

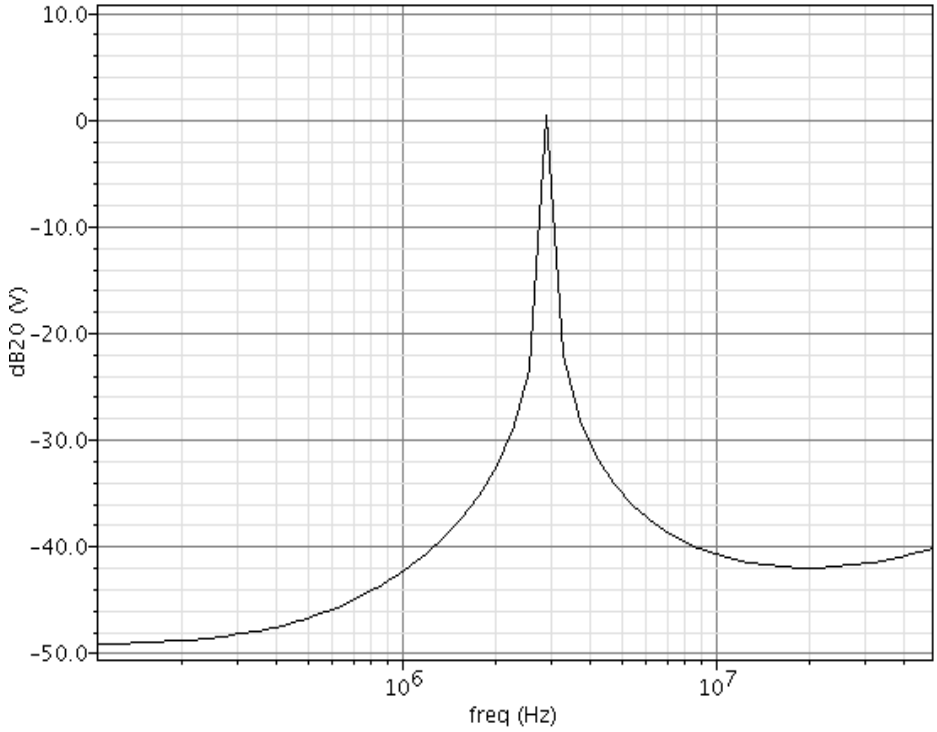


Fig. 7.18 Frequency spectrum of the proposed circuit in Fig. 4.5 (b)

The passive components values R_1 = 100 Ω, R_2 = 1.2 kΩ, R_3 = 600 Ω, R_4 = 5.5 kΩ, C_1 = 100 pF and C_3 = 100 pF are chosen to simulate the proposed circuit in Fig. 4.5 (b). Fig. 7.17 represents the simulated output waveform of the proposed circuit in Fig. 4.5 (b) with a frequency of 2.9 MHz. The simulated frequency in Fig. 7.17 is very close to the theoretical frequency of 3.21 MHz. The frequency spectrum for the proposed circuit in Fig. 4.5 (b) is shown in Fig. 7.18.

7.3 QUADRATURE SINUSOIDAL OSCILLATORS

7.3.1 SIMULATION RESULTS

The following passive components values are chosen to simulate the proposed circuit in Fig. 4.6, C_2 = 10 nF, C_4 = 100 nF, R_3 = 100 Ω, R_5 = 1 kΩ, R_4 = 7 kΩ and R_1 = 200 Ω. Fig. 7.19 represents the simulated output waveform of the proposed quadrature oscillator circuit with a frequency of 16.8 kHz. The variation of oscillation frequency with respect to the passive component C_2 is sown in Fig. 7.20. For Fig. 7.20, the following passive component values are chosen R_1 = 200 Ω, R_3 = 100 Ω, R_4 = 7 kΩ, R_5 = 1 kΩ, C_4 = 100 nF and C_2 is varied from 1 nF to 10 nF.

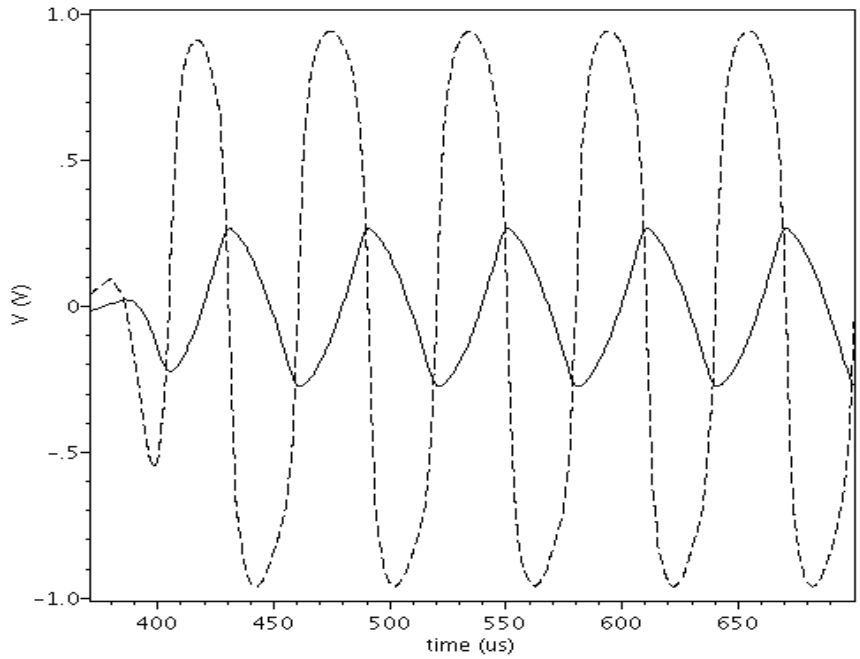


Fig. 7.19 Simulated output waveform of the proposed quadrature oscillator circuit in Fig. 4.6

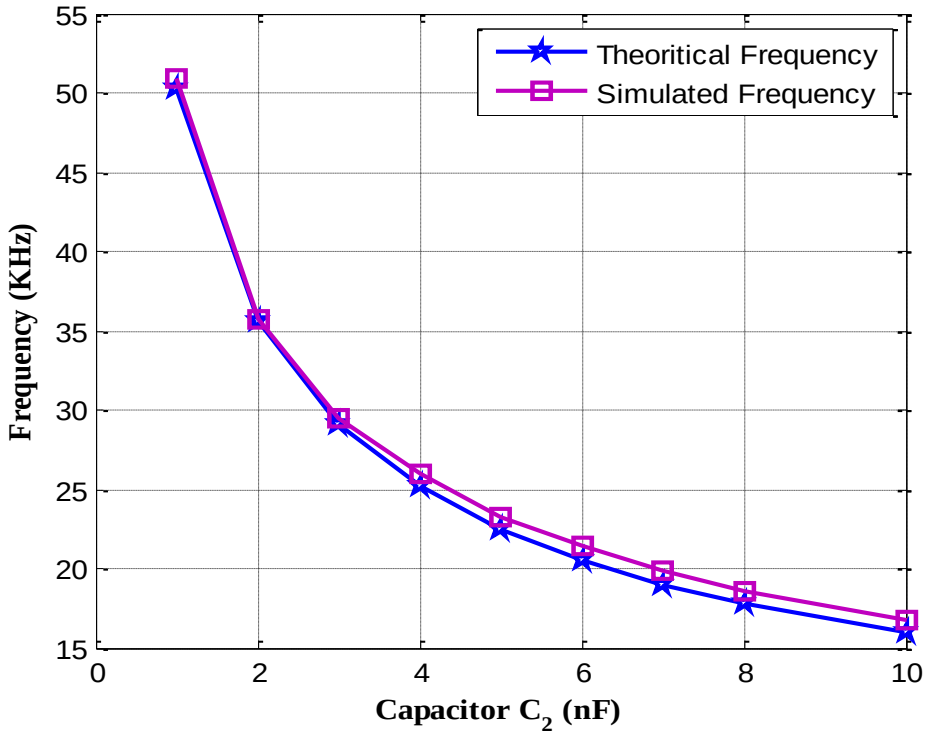


Fig. 7.20 Tunability of the proposed circuit in Fig. 4.6 with respect to the capacitor C_2

The proposed circuit in Fig. 4.7 is connected with the passive componens values, R_1 = 9 kΩ , R_2 = 500 Ω, R_3 = 1 kΩ, R_5 = 100 Ω, C_1 = 100 pF and C_4 = 100 pF. The simulated output waveform with a frequency of 2.4 MHz is shown in Fig. 7.21.

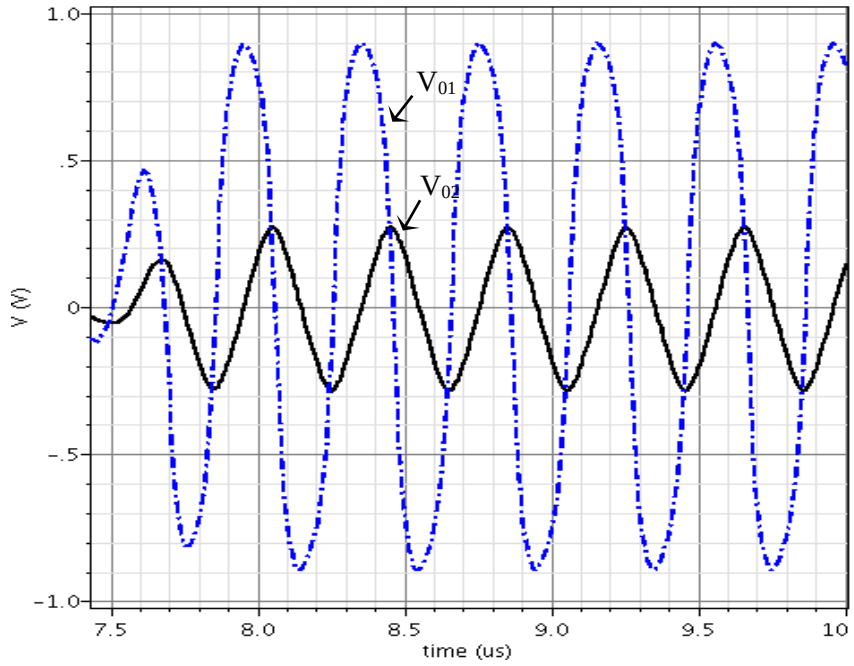


Fig. 7.21 Simulated output waveform of the proposed circuit in Fig. 4.7

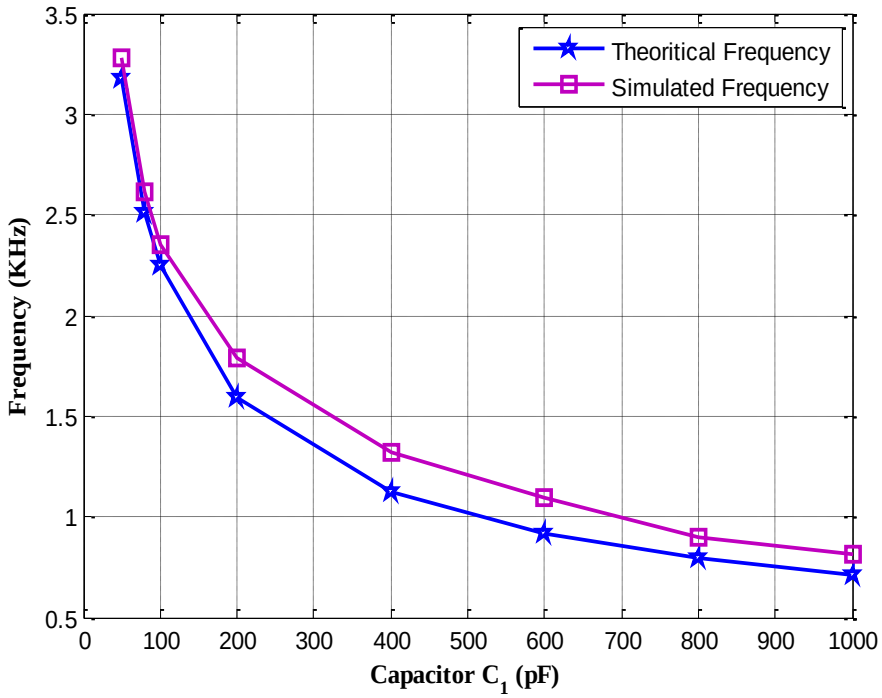


Fig. 7.22 Tunability of the proposed circuit in Fig. 4.7 with respect to the capacitor C_1

The variation of oscillation frequency with respect to the capacitor C_1 is shown in Fig.7.22. For this plot, the capacitor is varied from 50 pF to 1nF. The output voltages V_{01}versus V_{02} is shown in Fig. 7.23.

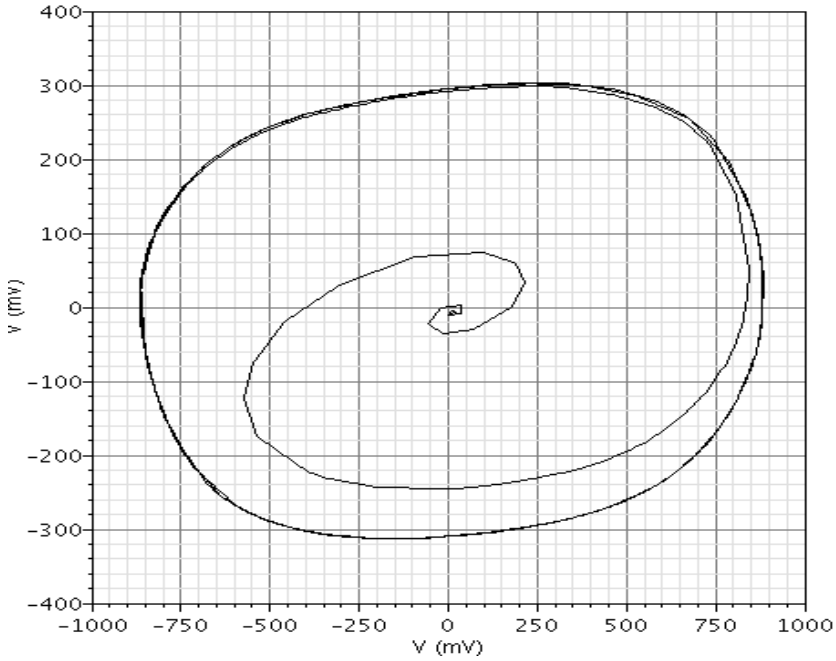


Fig. 7.23 Outputs V_{01} Vs V_{02} of the proposed circuit in Fig. 4.7

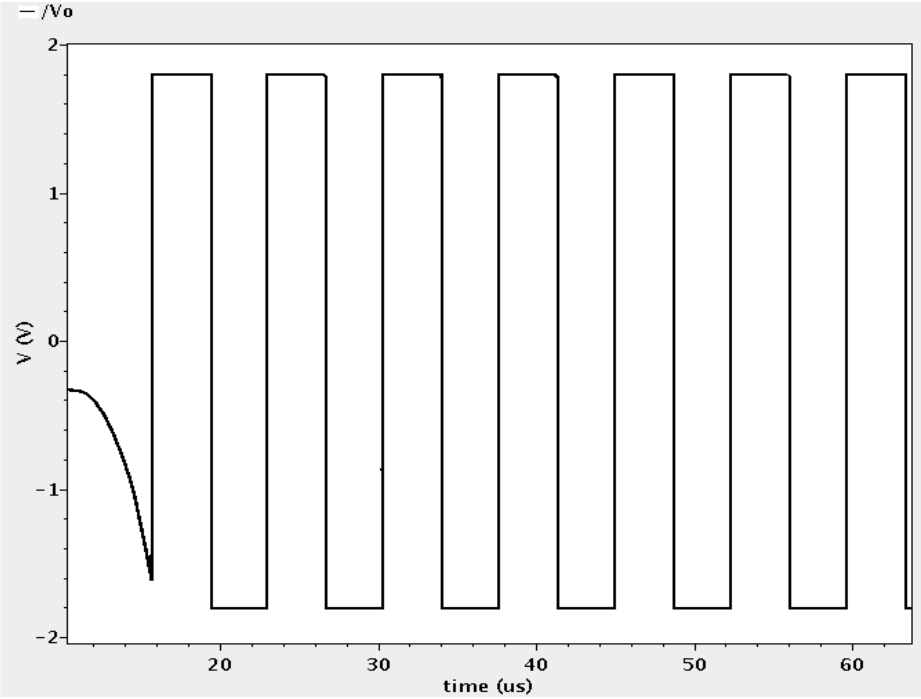
7.4 SQUARE WAVEFORM GENERATORS

7.4.1 SIMULATION RESULTS

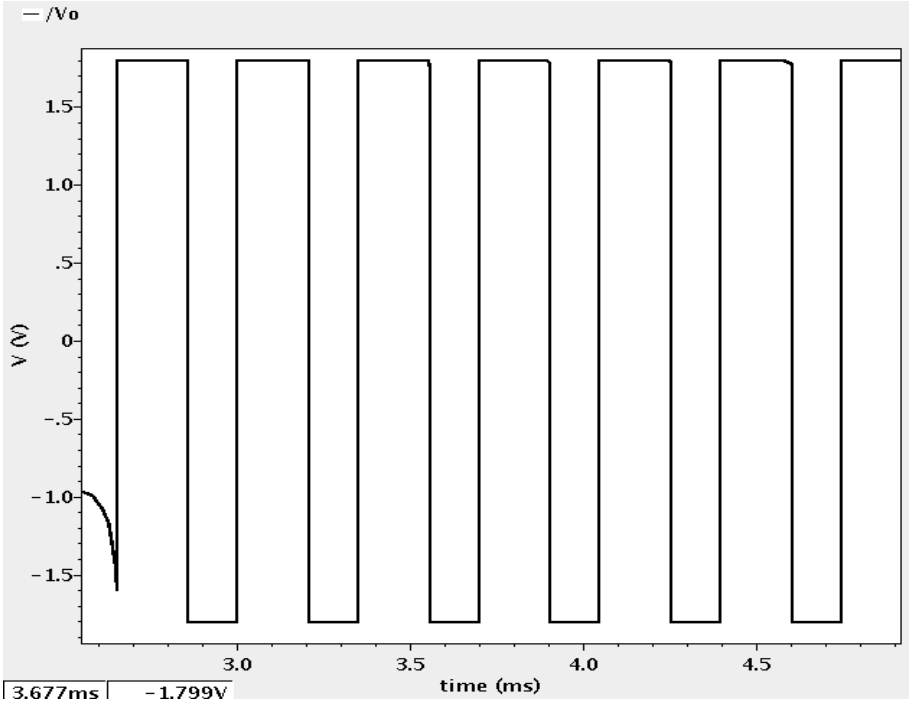
The simulated output results of the proposed square waveform generator circuits are given in Fig. 7.24. For generating the square-wave of the first proposed circuit in Fig. 4.8 (a), the required time period or frequency is chosen first. Then the ratio of R_1/R_2 is taken care of and the value of capacitor C is arbitrarily determined from the time period or frequency expression given in equation (5.46) or (5.47). For the proposed circuit shown in Fig. 4.8 (a), the required time period is chosen as 0.71 μs. The passive components chosen for the proposed circuit shown in Fig. 4.8 (a) are R_1 = 15 kΩ, R_2 = 1.5 kΩ and C = 10 pF. However, with this circuit the on-duty and off-duty cycles are fixed as shown in Fig. 7.24 (a). For the second proposed circuit in Fig. 4.8 (b), the values of resistors $R_1 = R_{11} = R_{12}$, R_2 and capacitor C are derived from the above process as stated in fixed duty cycles.

Then the resistors R_{11} and R_{12} are tuned independently to set the required on-duty and off-duty cycles. If resistor R_{11} is chosen greater than the resistor R_{12}, then the on-duty cycle is more than the off-duty cycle. These values will be ($R_{12} > R_{11}$) reversed to set the off-duty cycle more than the on-duty cycle. The required time

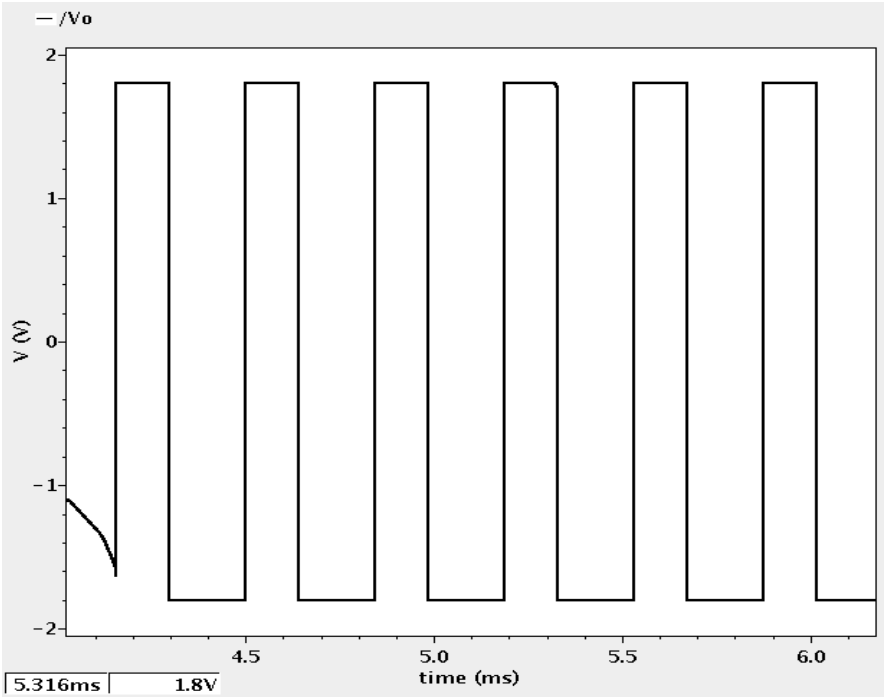
period is chosen as 0.32 ms. The passive components R_2 = 1.5 kΩ R_{11} = 1.5 kΩ, R_{12} = 5 kΩ and C = 0.1 nF are used to simulate the proposed circuit with 60% on duty cycle and 40% off-duty cycle. The corresponding simulated output waveforms for the second proposed circuit are given in Fig. 7.24 (b) and (c).



(a) Output waveform of the first proposed circuit (T_{ON} =T_{OFF})



(b) Output waveform of the second proposed circuit (T_{ON} > T_{OFF})



(c) Output waveform of the second proposed circuit ($T_{ON} < T_{OFF}$)

Fig. 7.24 Output waveforms of the proposed square-wave generators

The tunability of time period with respect to resistor R_2 is shown in Fig. 7.24. For the tenability plot, the passive components R_1 = 15 kΩ and C = 1 nF are used, R_2 is varied from 200 Ω to 3 kΩ.

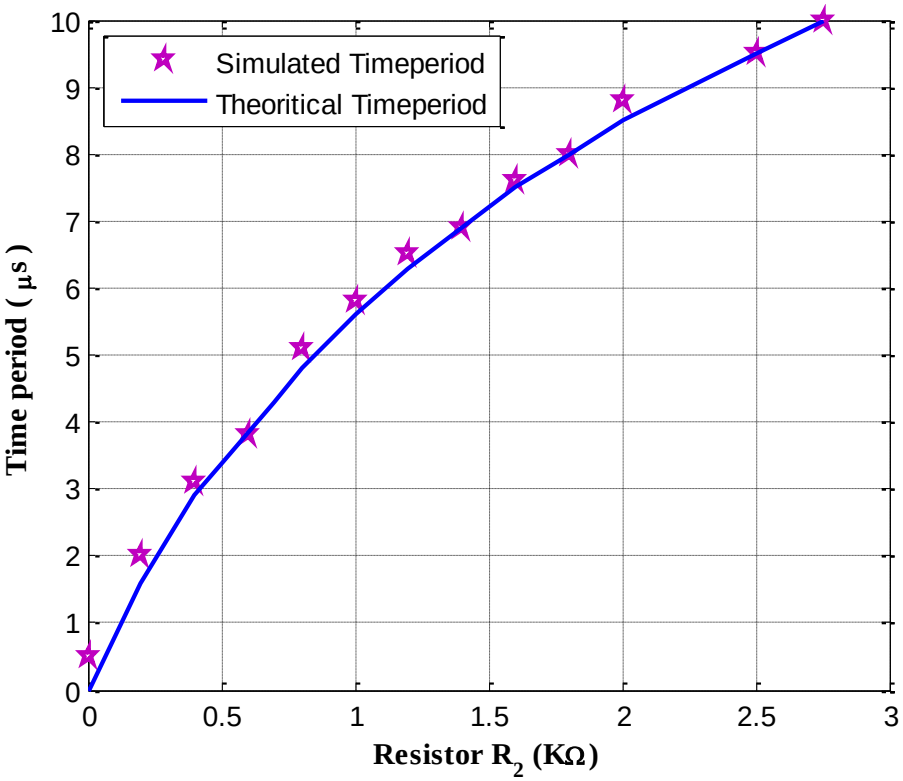


Fig. 7.25 Tunability of time period against resistor R_2

7.5 SUMMARY

The simulation results are presented in this chapter to validate the mathematical analysis given in chapter 5. All the proposed circuits are simulated using Spectre simulation model parameters with a supply voltage of ± 1.8 V. The simulated output waveforms of all the proposed circuits are presented in this chapter. For all the proposed circuits the passive component values are given to validate the theoretical analysis. The simulation frequencies of all the proposed circuits are matched with the theoretically calculated frequencies from chapter 5.

CHAPTER 8

HARDWARE IMPLEMENTATION

8.1 INTRODUCTION

In this chapter, the experimental results for the proposed circuits in chapter 4 are given. All the proposed circuits are tested for waveform generation on a laboratory breadboard by using a prototype OTRA circuit. The prototype OTRA circuit is designed by using two AD 844 AN ICs [45-49]. The IC AD 844 AN is a high speed monolithic current feed-back operational amplifier (CFOA). This IC is used in many applications and it can be used in place of traditional op-amps to get much better AC performance and high linearity. The AD 844 AN is very popular by its applications in current-mode circuits. By using this IC many active current-mode devices can be implemented on a laboratory breadboard like second generation current conveyor (CCII), operational transconductance amplifier (OTA), current differencing buffered amplifier (CDBA), current differencing transconductance amplifier (CDTA) and second generation differential current conveyor (DCCII).

The main advantages of using AD 844 AN in current-mode applications, the closed-loop bandwidth is independent of the closed-loop gain and free from the slew rate limitations. To investigate the proposed circuits for waveform generation and frequency tuning with respect to the passive components connected to the circuits, the equivalent prototype circuit model of the OTRA shown in Fig. 2.14 with two AD 844 AN ICs is used. For the OTRA prototype circuit ± 5 V supply voltages are used to produce the oscillations in all the proposed circuits in chapter 4.

8.2 GROUNDED RESISTANCE/CAPACITANCE SINUSOIDAL OSCILLATORS

8.2.1 EXPERIMENTAL RESULTS

The circuits shown in Fig. 4.3 and 4.4 are generated from the generalized configuration shown in Fig. 4.2. These circuits' passive components are connected externally to the inverting and non-inverting terminal of the equivalent circuit model of OTRA shown in Fig. 8.1 on a laboratory breadboard. For the first proposed

minimum component oscillator circuit shown in Fig. 4.3, the passive components R_1 = 10 Ω, R_3 = 1 kΩ, C_2 = 10 nF and C_4 = 1 nF have been used to generate the oscillation.

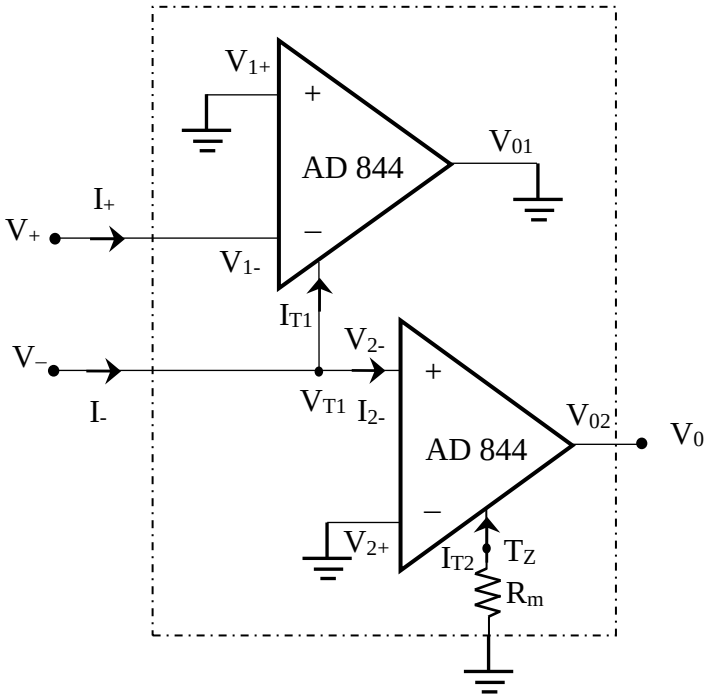
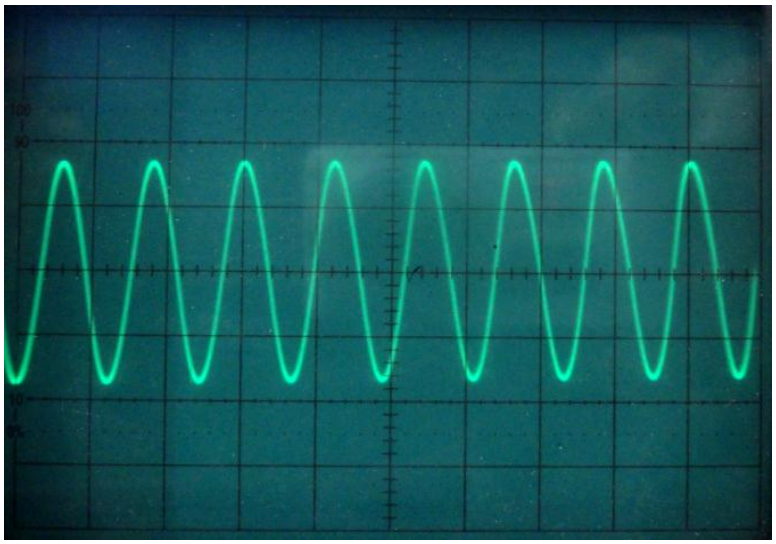


Fig. 8.1 Implementation of OTRA using AD 844 ICs

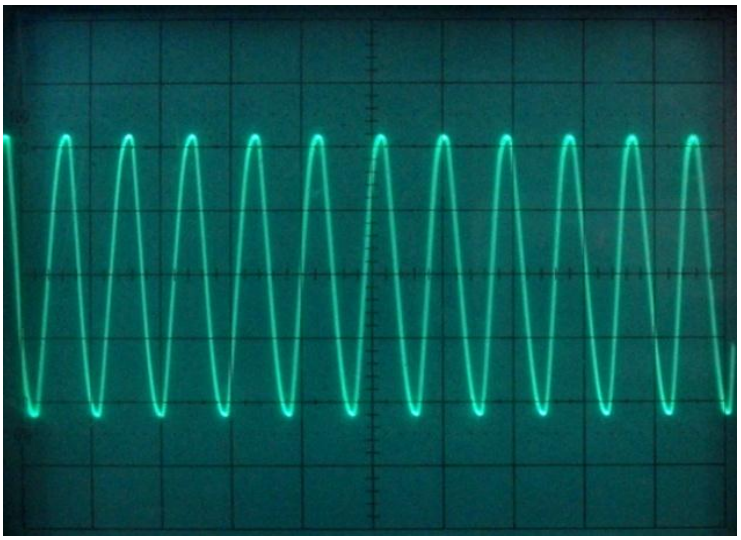
The corresponding output waveform of the proposed oscillator circuit is shown in Fig. 8.2. The experimental oscillation frequency of the oscillator circuit in Fig. 4.3 is 15.3 kHz, which is close to the theoretical value of 15.9 kHz.



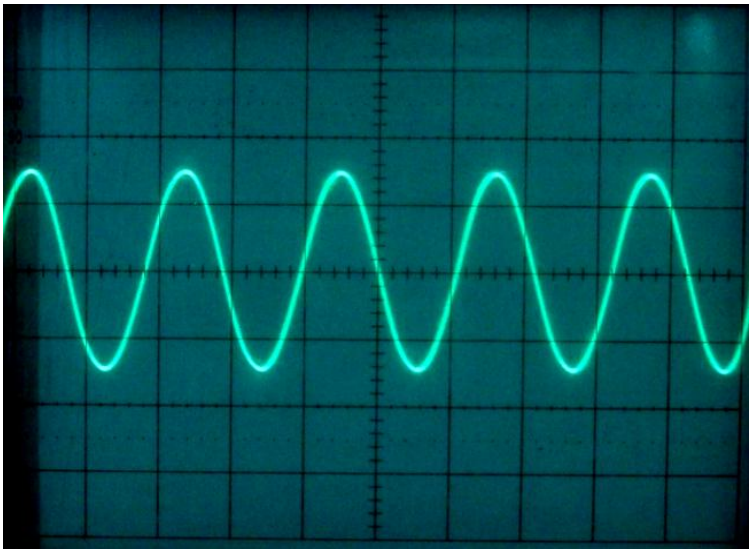
Scale: X-axis 50 μs/div and Y-axis 1 V/div.

Fig. 8.2 Experimental output waveform of the proposed circuit shown in Fig. 4.3

A typical waveform from the oscilloscope screen for the proposed circuit in Fig. 4.4 (a) is presented in Fig. 8.3, which have been obtained for the passive components R_3 = 60 Ω, R_5 = 1 kΩ, R_7 = 300 Ω, C_2 = 10 nF and C_4 = 100 nF. The measured frequency of 22.2 kHz, as shown in Fig. 8.3, which is close to the theoretical result of 22.45 kHz. The percentage of error between the theoretical and practical oscillation frequency is 1.02 %.



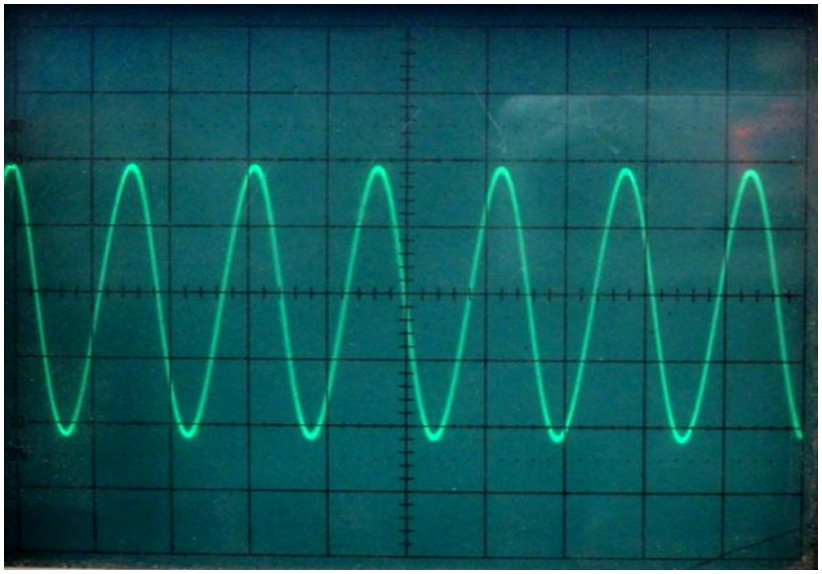
Scale: X-axis 50 µs/div and Y-axis 1 V/div.
Fig. 8.3 Output waveform of the proposed circuit in Fig. 4.4 (a)



Scale: X-axis 50 µs/div and Y-axis 1 V/div.
Fig. 8.4 Output waveform of the proposed circuit in Fig. 4.4 (b)

The proposed oscillator circuit shown in Fig. 4.4 (b), is designed with the passive components C_1 = 100 nF, C_4 = 100 nF, C_7 = 100 nF, R_3 = 150 Ω and R_5 = 500

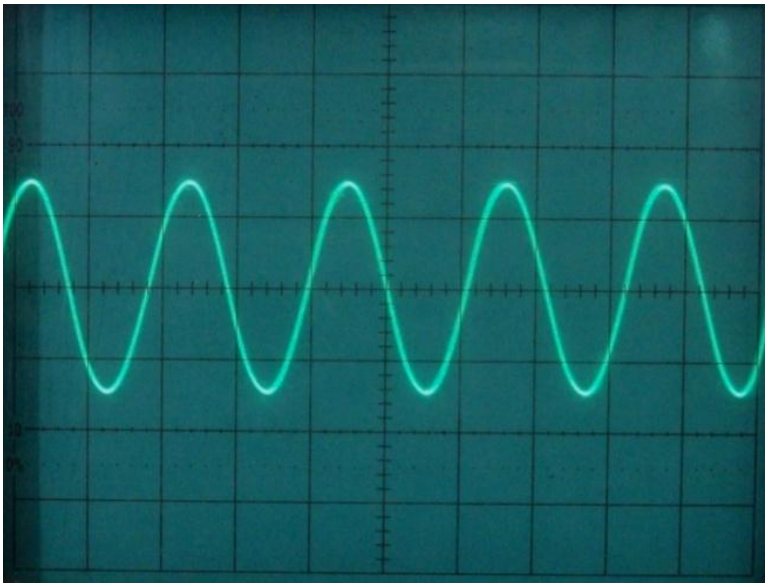
Ω on a laboratory breadboard. Figure 8.4 represents the output waveform of the proposed circuit shown in Fig. 4.4 (b). From Fig. 8.4, the oscillation frequency of the second proposed oscillator circuit stands at 5 kHz, which is close to the theoretical value of 5.78 kHz.



Scale: X-axis 5 µs/div and Y-axis 1 V/div.
Fig. 8.5 Output waveform of the proposed circuit shown in Fig. 4.4 (c)

The passive components, R_1 = 1 kΩ, R_3 = 150 Ω, R_7 = 15 Ω, C_5 = 1 nF and C_6 = 10 nF are used to design the proposed oscillator circuit shown in Fig. 4.4 (c). The corresponding output waveform on the oscilloscope for the proposed oscillator circuit shown in Fig. 4.4 (c) is given in Fig. 8.5. The experimental oscillation frequency of the oscillator circuit is 125 kHz, which is close to the theoretical value of 129.3 kHz.

The proposed circuit shown in Fig. 4.4 (d) is constructed with the passive components R_2 = 500 Ω, R_3 = 12 kΩ, R_5 = 400 Ω, R_7 = 2 kΩ, C_4 = 10 nF and C_6 = 1 nF on a laboratory breadboard. Fig. 8.6 describes the output waveform of the oscillator circuit with a frequency of 23.8 kHz, whereas, the theoretical oscillation frequency is 27.02 kHz. The tunability of the proposed circuit is checked with the passive components R_2 = 500 Ω, R_3 = 12 kΩ, R_5 = 400 Ω, C_4 = 10 nF, C_6 = 1 nF and R_7 is varied from 1 kΩ to 10 kΩ. The variation of oscillation frequency with respect to the resistor R_7 is shown in Fig. 8.7. For producing the oscillations in the proposed oscillator circuit as in Fig. 4.4 (e), the passive components R_2 = 1 kΩ, R_4 = 60 Ω, R_7 = 50 Ω, C_6 = 10 nF and C_3 = 100 nF are connected to the prototype OTRA circuit on a laboratory breadboard.



Scale: X-axis 50 µs/div and Y-axis 1 V/div
Fig. 8.6 Output waveform of the proposed circuit in Fig. 4.4 (d)

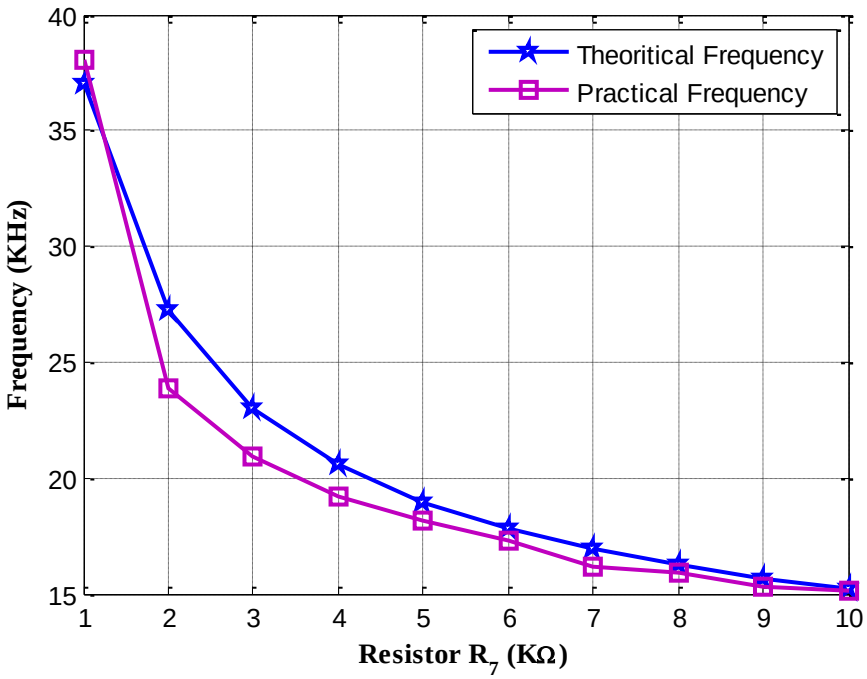
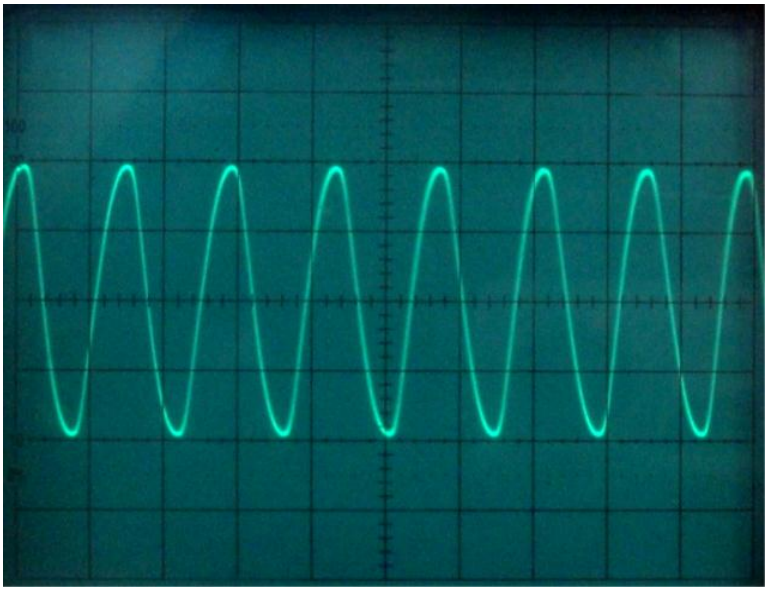


Fig. 8.7 Tunability of the proposed circuit in Fig. 4.4 (d) with respect to the resistor R_7

The experimental output waveform of the proposed circuit is given in Fig. 8.8 with a frequency of 35.7 kHz, whereas the theoretical oscillation frequency was calculated as 30.2 kHz. The variation of oscillation frequency with respect to the passive component connected to the circuit is shown in Fig. 8.9. For generating the variation of oscillation frequency figure, the passive components R_1 = 1 kΩ, R_4 = 60 Ω, C_6 = 10 nF and C_3 = 100 nF have been used and R_7 is varied from 700 Ω to 10 kΩ.



Scale: X-axis 20 µs/div and Y-axis 1 V/div.
Fig. 8.8 Output waveform of the proposed circuit in Fig. 4.4 (e)

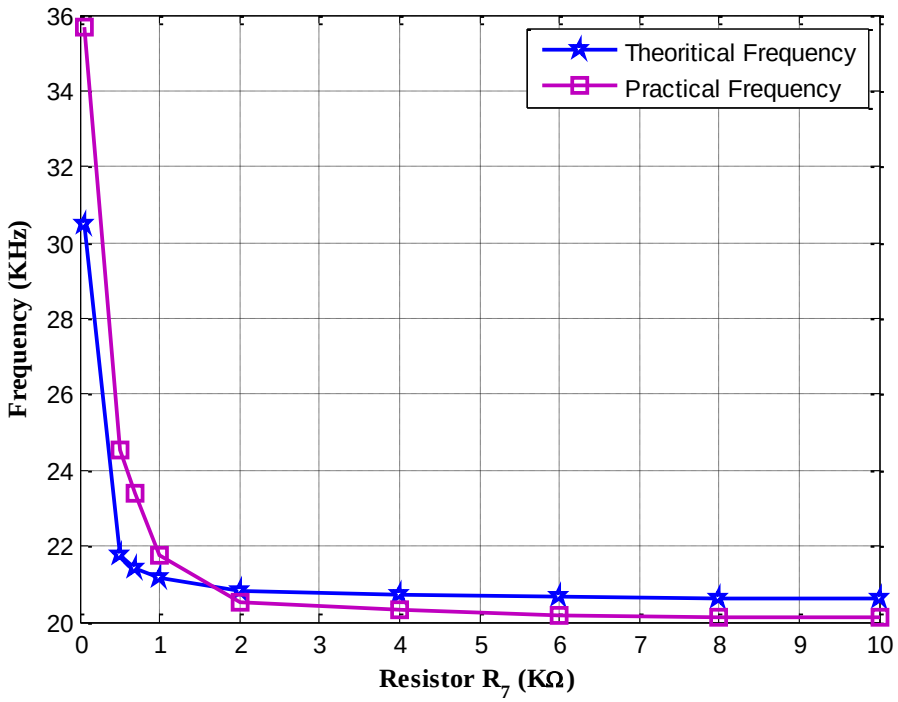
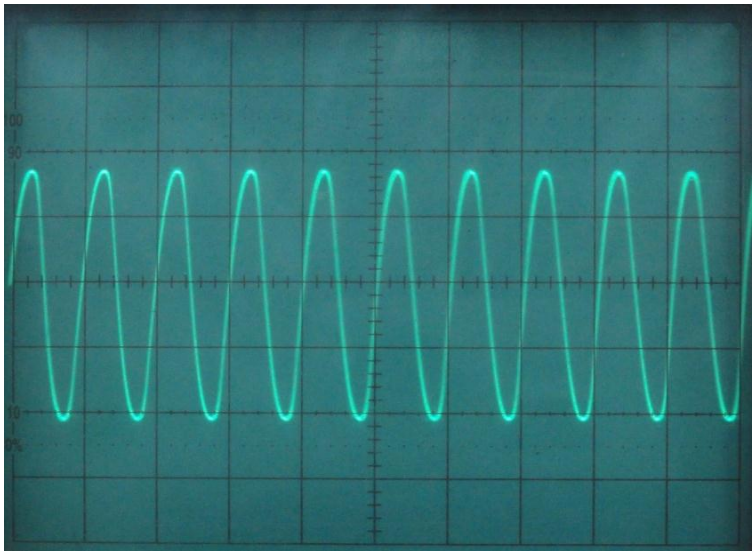


Fig. 8.9 Tunability of the proposed circuit in Fig. 4.4 (e) with respect to the resistor R_7

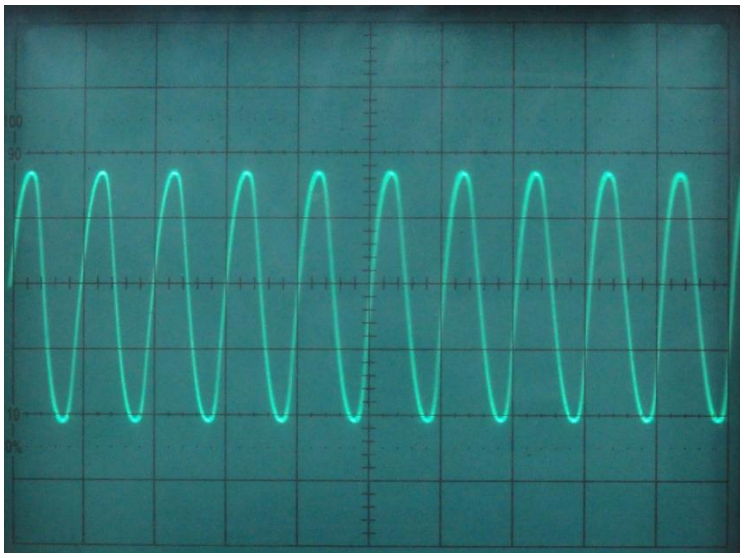
The Fig. 8.1 is connected with the external passive components C_2 = 10 nF, C_4 = 100 nF, R_3 = 100 Ω, R_5 = 1 kΩ, R_6 = 7 kΩ and R_7 = 200 Ω on a laboratory breadboard for generating the oscillations in the proposed circuit shown in Fig. 4.4 (f). The experimental output waveform of proposed circuit is given in Fig. 8.10 with a frequency of 18.18 kHz which is close to the theoretical result of 18.6 kHz.



Scale: X-axis 50 µs /div and Y-axis 2 V/div

Fig. 8.10 Experimental output wave form of the proposed circuit in Fig. 4.4 (f)

For generating the oscillations in the proposed circuit shown in Fig. 4.4 (g), the passive component values are chosen to be R_3 = 1 kΩ, R_6 = 1 kΩ, R_7 = 5 kΩ, C_2 = 100 nF and C_4 = 100 nF. Figure 8.11 represents the experimental output waveform of the proposed circuit with a frequency of 19 kHz which is close to the theoretical result of 20 kHz.

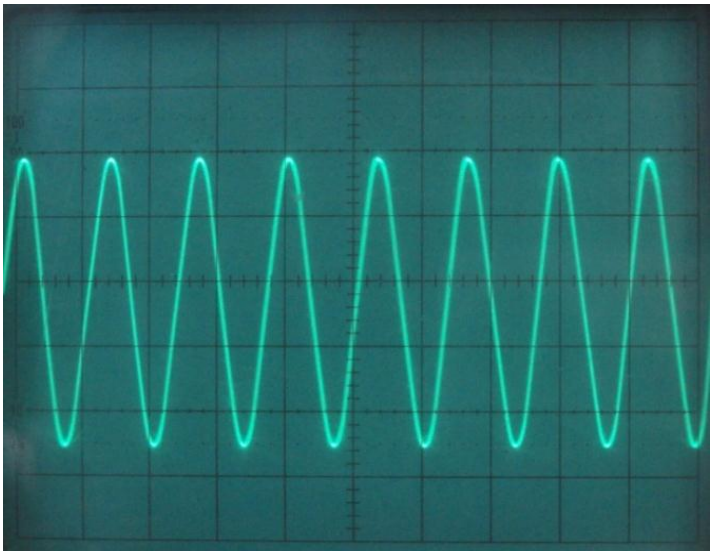


Scale: X-axis 50 µs /div and Y-axis 2 V/div

Fig. 8.11 Experimental output wave form of the proposed circuit in Fig. 4.4 (g)

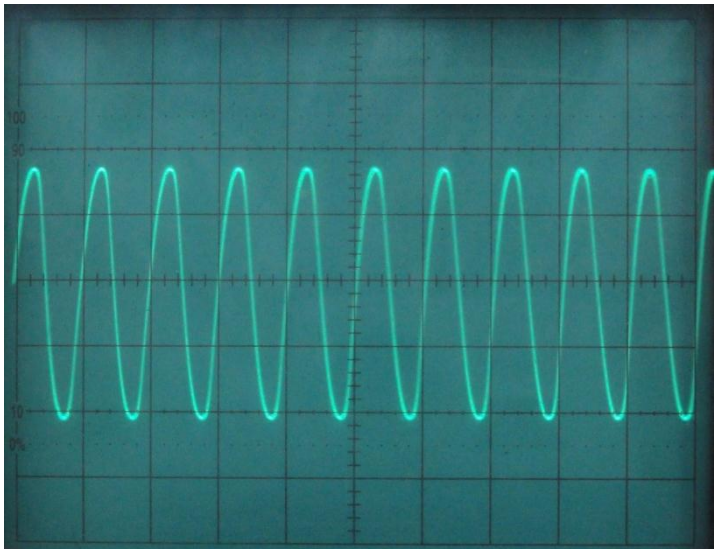
The passive component values C_1 = 100 nF, C_3 = 100 nF, R_2 = 50 Ω and R_4 = 500 Ω are used for the proposed circuit shown in Fig. 4.4 (h) to generate oscillations.

The experimental output waveform of the proposed circuit in Fig. 4.4 (h) is given in Fig. 8.12.



Scale: X-axis 50 µs/div and Y-axis 2 V/div
Fig. 8.12 Experimental output wave form of the proposed circuit in Fig. 4.4 (h)

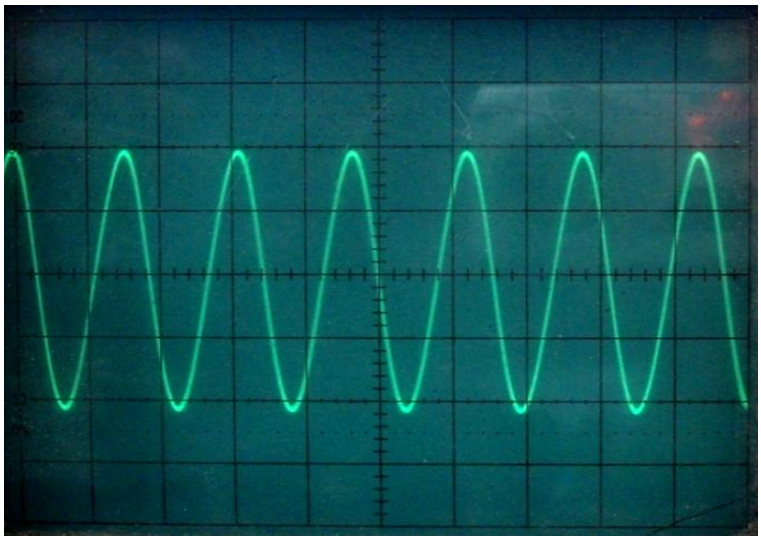
Likewise, the passive components values C_1 = 10 nF, C_2 = 100 nF, R_3 = 100 Ω and R_5 = 5 kΩ are used on a laboratory breadboard for generating the oscillations in the proposed circuit shown in Fig. 4.4 (i). The experimental output waveform of the proposed circuit in Fig. 4.4 (h) is given in Fig. 8.13.



Scale: X-axis 50 µs /div and Y-axis 2 V/div
Fig. 8.13 Experimental output wave form of the proposed circuit in Fig. 4.4 (i)

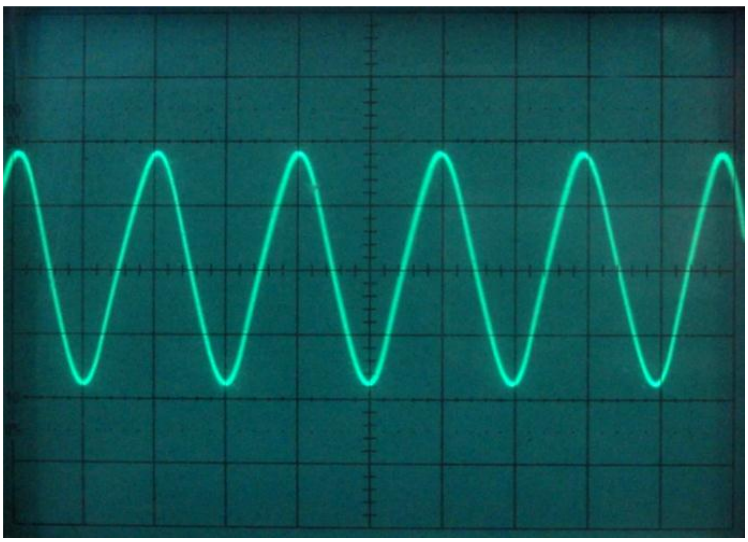
The following passive components values are chosen for the proposed circuit in Fig. 4.5 (a), R_1 = 100 Ω, R_2 = 1.2 kΩ, R_3 = 600 Ω, R_4 = 5.5 kΩ, C_2 = 10 nF and C_3 =

100 nF. Figure 8.14 represents the experimental output waveform of the proposed circuit in Fig. 4.5 (a) with a frequency of 10.3 kHz, which is close to the theoretical value of 10 kHz.



Scale: X-axis 50 μs/div and Y-axis 1 V/div.
Fig. 8.14 Experimental output waveform of the proposed circuit in Fig. 4.5 (a).

Similarly, the proposed circuit shown in Fig. 4.5 (b) is connected on a laboratory breadboard with the following external passive components R_1 = 100 Ω, R_2 = 1.2 kΩ, R_3 = 600 Ω, R_4 = 5.5 kΩ, C_2 = 10 nF and C_3 = 100 nF. The experimental output waveform is depicted in Fig. 8.15.



Scale: X-axis 20 μs/div and Y-axis 1 V/div.
Fig. 8.15 Experimental output waveform of the proposed circuit in Fig. 4.5 (b)

The comparative analysis of the proposed oscillator and quadrature oscillator circuits shown in Fig. 4.4 (a) and Fig. 4.6 with the existing oscillator circuits in the literature is shown in the Table 8.1.

TABLE 8.1 Comparison of the proposed circuit in Fig. 4.4 (a) and 4.6 with the conventional sinusoidal oscillators in the literature

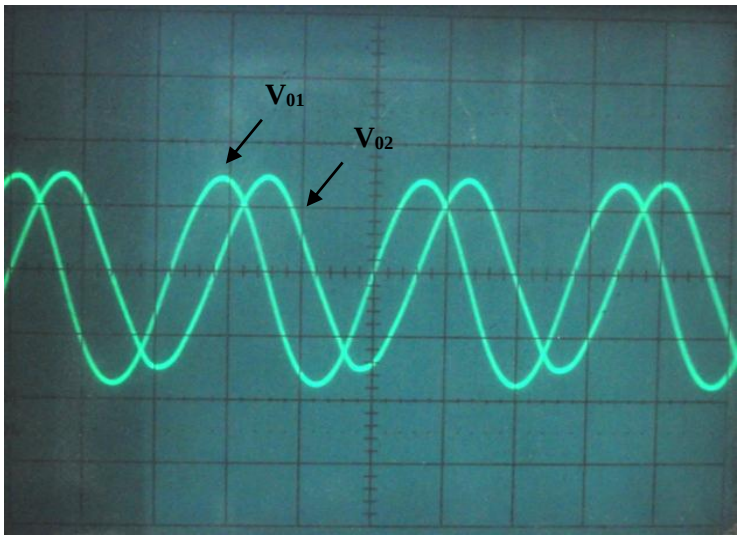
Oscillator circuits	Number of active components	Total number of resistors	Total number of capacitors	Total number of components	Supply voltage (V)	Power consumption (mW)
[21]	2 CCII	2	2	6	± 9	278.4
[22]	2 CCII	3	4	9	± 15	≈ 600
[30] Fig. 4	2 CCII	4	3	9	± 9	520
[29] Fig. 1 (a)	3 CFOA	4	2	9	± 12	648
[50] Fig. 4	2 OTRA	4	2	8	± 5	250.8
[50] Fig. 5 (a) & 5 (b)	2 OTRA	4	2	8	± 5	250.2
[51]	1 OTRA	3	2	6	± 5	114.2
[52] Fig. 4 (a)	1 OTRA	2	2	5	± 5	106.3
Proposed circuit in Fig. 4.4 (a)	1 OTRA	2	2	5	± 5	106.2
Proposed circuit in Fig. 4.6	2 OTRA	4	2	8	± 5	250.4

8.3 QUADRATURE SINUSOIDAL OSCILLATORS

8.3.1 EXPERIMENTAL RESULTS

For generating the oscillations of the proposed circuits shown in Fig. 4.6 and 4.7 on a laboratory breadboard, the OTRA equivalent circuit shown in Fig. 8.1 is connected with external passive components. The quadrature oscillator circuit shown in Fig. 4.6 is connected with the passive components C_2 = 10 nF, C_4 = 100 nF, R_3 =

100 Ω, R_5 = 1 kΩ, R_4 = 7 kΩ and R_1 = 200 Ω to generate the oscillations with 90° phase shift. The corresponding output waveforms of V_{01} and V_{02} on oscilloscope screen are shown in Fig. 8.16.



Scale: X-axis 20 µs /div and Y-axis 1 V/div

Fig. 8.16 Experimental output waveform for the proposed circuit in Fig. 4.6

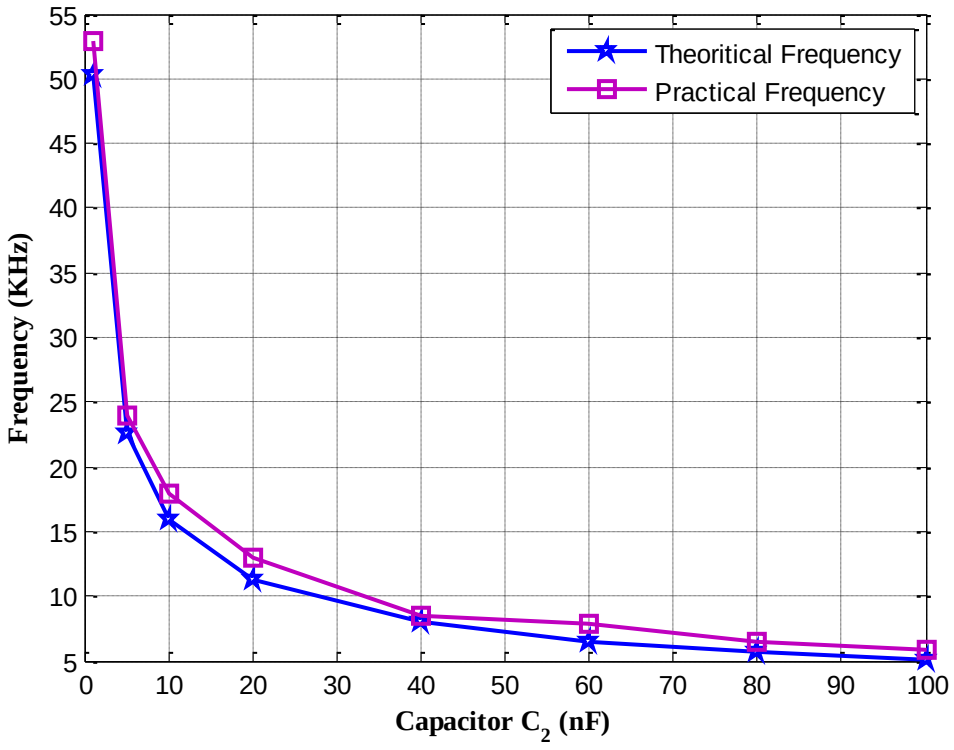


Fig. 8.17 Tunability of the proposed circuit in Fig. 4.6 with respect to the capacitor C_2

The variation of oscillation frequency with respect to the passive component C_2 is shown in Fig. 8.17. For this figure, the passive components C_4 = 100 nF, R_3 = 100 Ω,

R_5 = 1 kΩ, R_4 = 7 kΩ and R_1 = 200 are used and C_2 is varied form 1 nF to 100 nF. The lissajous curves of the output voltages V_{01} verses V_{02} is shown in Fig. 8.18.

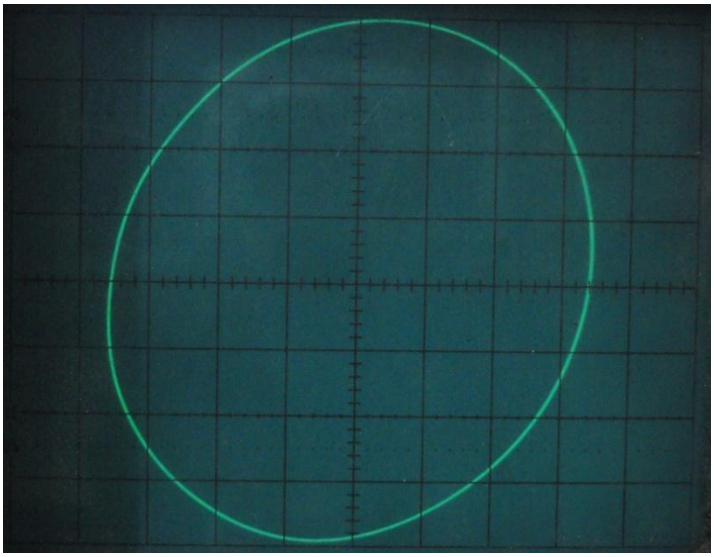
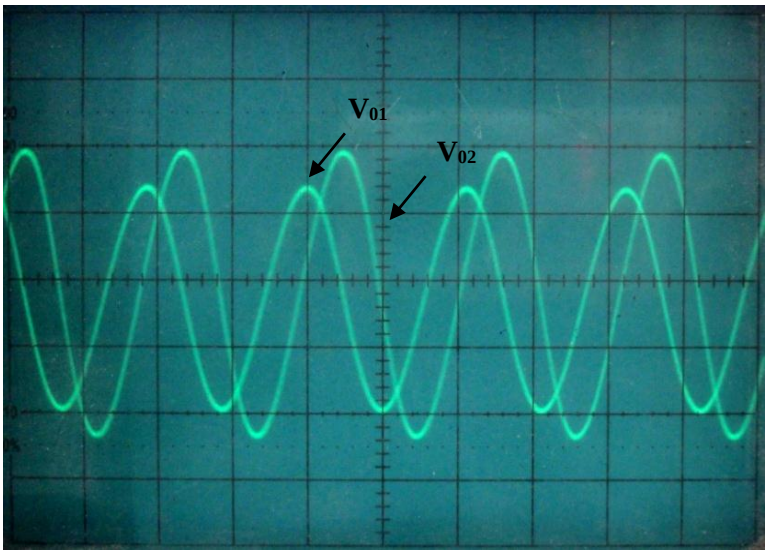


Fig. 8.18 The voltages V_{01} versus V_{02} of the proposed quadrature oscillator on oscilloscope



Scale: X-axis 20 μs/div and Y-axis 1 V/div
Fig. 8.19 Experimental output waveform of the proposed circuit in Fig. 4.7

Similarly, the proposed circuit shown in Fig. 4.7 is connected with the passive components R_1 = 9 kΩ, R_2 = 500 Ω, R_3 = 1 kΩ, R_5 = 100 Ω, C_1 = 10 nF and C_4 = 10 nF on a laboratory breadboard for waveform generation. The output waveforms at the output terminals V_{01} and V_{02} of the OTRAs in Fig 4.7 is shown in Fig. 8.19. The variation of oscillation frequency with respect to the capacitor C_1 is shown in Fig. 8.20. For this figure, the passive components R_1 = 9 kΩ , R_2 = 500 Ω, R_3 = 1 kΩ, R_5 = 100 Ω,

and C_4 = 10 nF have been used and C_1 is varied from 1 nF to 100 nF. The lissajous curves between the output voltages V_{01} verses V_{02} is shown in Fig. 8.21.

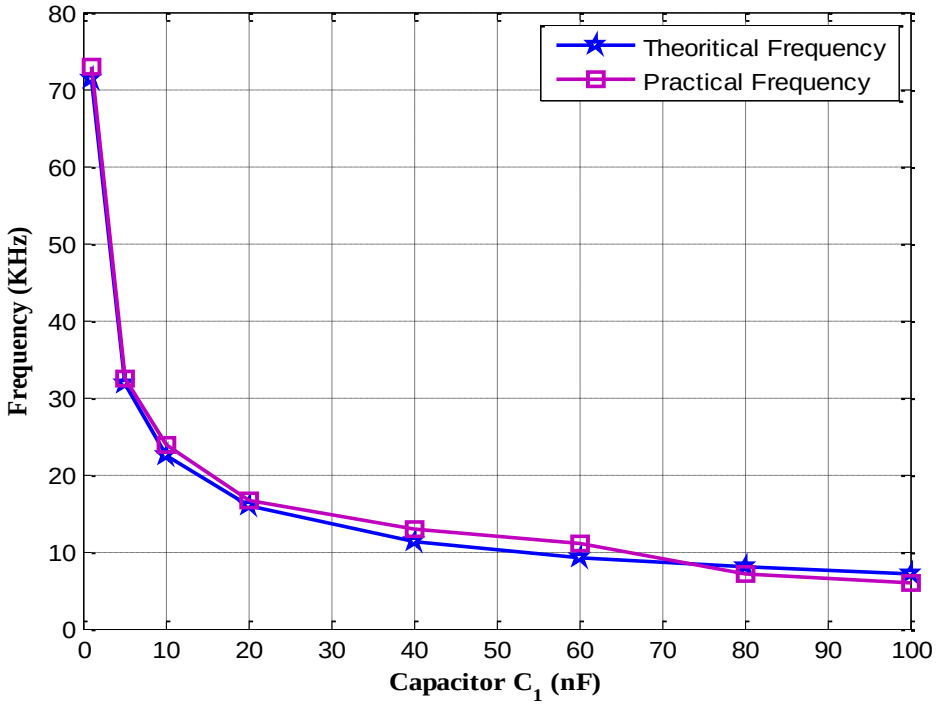


Fig. 8.20 Tunability of the proposed circuit in Fig. 4.6 with respect to the capacitor C_1

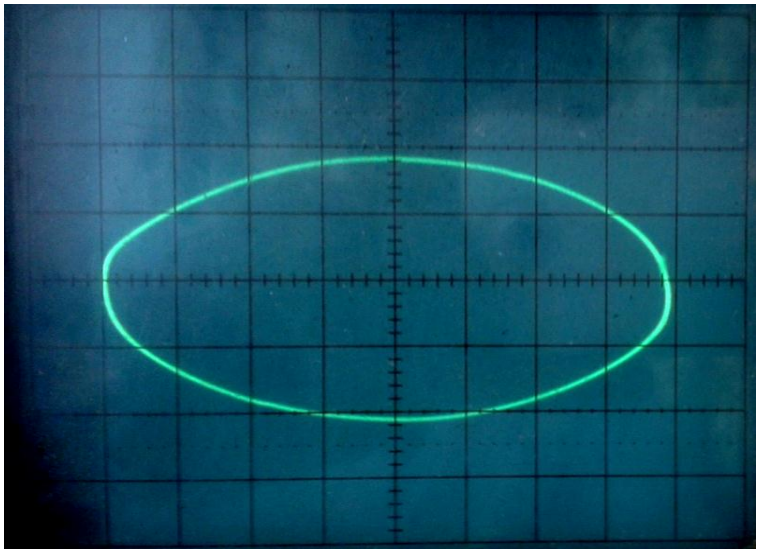
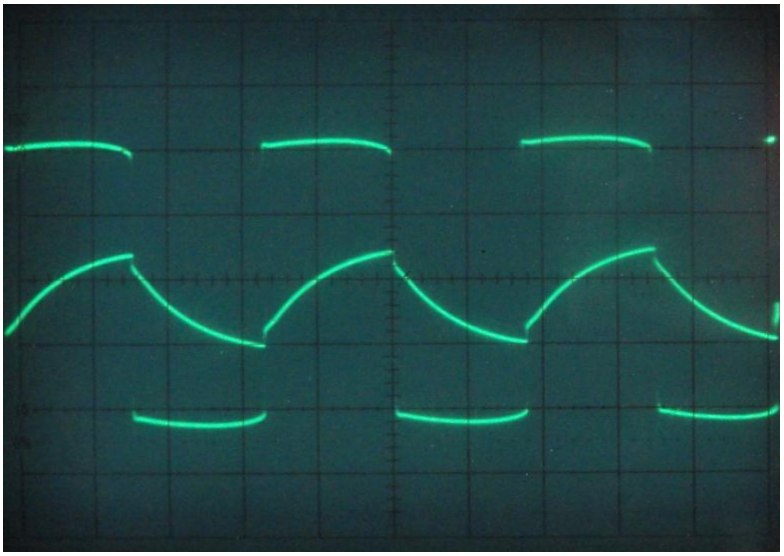


Fig. 8.21 The voltage V_{01} versus V_{02} of the proposed quadrature oscillator on oscilloscope

8.4 SQUARE WAVEFORM GENERATORS

8.4.1 EXPERIMENTAL RESULTS

For the proposed square waveform generator circuit shown in Fig. 4.8 (a), the required time period is chosen first. Then, suitable values of passive components (R_1, R_2 and C) are derived from the time period or frequency equations (5.46) or (5.47). For higher sensitivity of the time period with respect to the resistor, the resistor R_2 is chosen to be less than 2 kΩ. For example, if the required time period is 7.19 µs, then R_1, R_2 and C values are chosen to be 15 kΩ, 1.5 kΩ and 1 nF. The proposed circuit shown in Fig. 4.8 (a) is connected on a laboratory breadboard with the help of the OTRA equivalent model shown in Fig. 8.1 and the selected passive components. The experimental output waveform of the proposed circuit shown in Fig. 4.8 (a) is given in Fig. 8.22 with a time period of 7.02 µs.

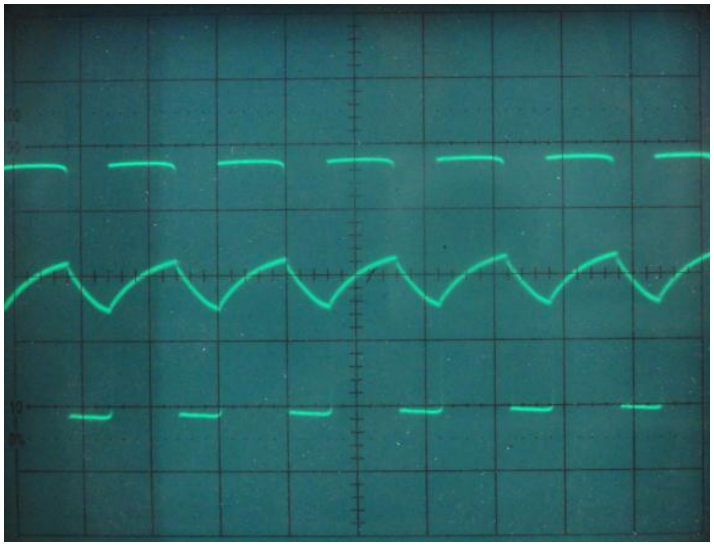


Scale: X-axis 2 µs/div and Y-axis 2 V/div.

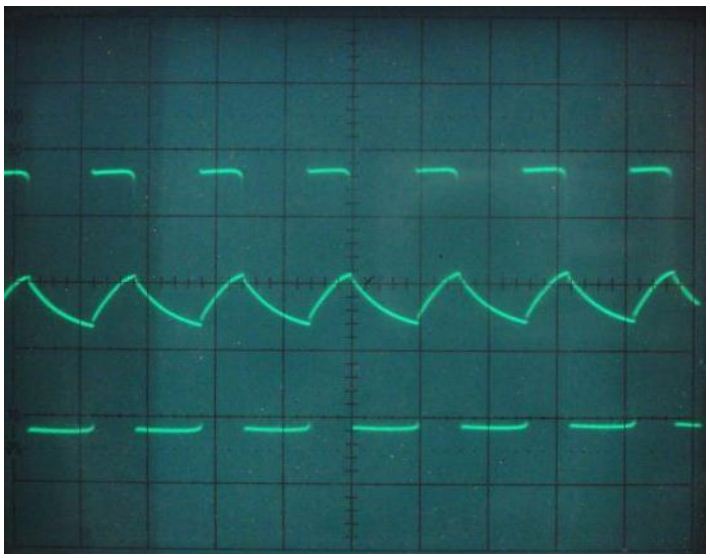
Fig. 8.22 Output waveform with almost equal and fixed duty cycles ($T_{ON} = T_{OFF}$)

Similarly, in the case of second proposed circuit shown in Fig. 4.8 (b), the suitable passive component values will be obtained from the equation (5.53) or (5.54) for a selected time period. If the required time period is 0.32 ms with 60 % on-duty and 40 % off-duty cycles. The resistors and capacitor values chosen to set the required time period are R_2 = 1.5 kΩ R_{11} = 1.5 kΩ, R_{12} = 5 kΩ and C = 0.1 nF. The capacitor C is slightly increased to set the required time period. The resistor R_{11} and R_{12} values will be reversed to set the 40 % on-duty and 60 % off-duty cycles.

The output waveform with 60 % on-duty and 40 % off-duty cycle for the second proposed circuit is shown in Fig. 8.23 (a). Likewise, the passive components R_2 = 1.5 kΩ, R_{11} = 5 kΩ, R_{12} = 1.5 kΩ and C = 0.1 nF are selected to get the 40 % on-duty and 60 % off-duty cycles with the proposed circuit shown in Fig. 4.8 (b).



Scale: X-axis 0.2 ms/div and Y-axis 5 V/div.
(a) Output waveform with variable on-duty cycle ($T_{ON} > T_{OFF}$)



Scale: X-axis 0.2 ms/div and Y-axis 5 V/div.
(b) Output waveform with variable off-duty cycle ($T_{ON} < T_{OFF}$)

Fig. 8.23 Experimental output waveforms of the second proposed circuit

The experimental output waveform with 40% on-duty and 60% off-duty cycle is shown in Fig. 8.23 (b). Several experiments are performed on a laboratory breadboard to test the tunability of the proposed circuits shown in Fig. 4.8 (a) and (b) against the passive components R_1, R_2 and C. The results are presented in Figs. 8.24 - 8.26 for the

proposed circuit configuration shown in Fig. 4.8 (a). For all measurements on tunability, the supply voltage of ± 5 V is used. Figures 8.24, 8.25 and 8.26 denote the time period variation against the passive components R_1, R_2 and C.

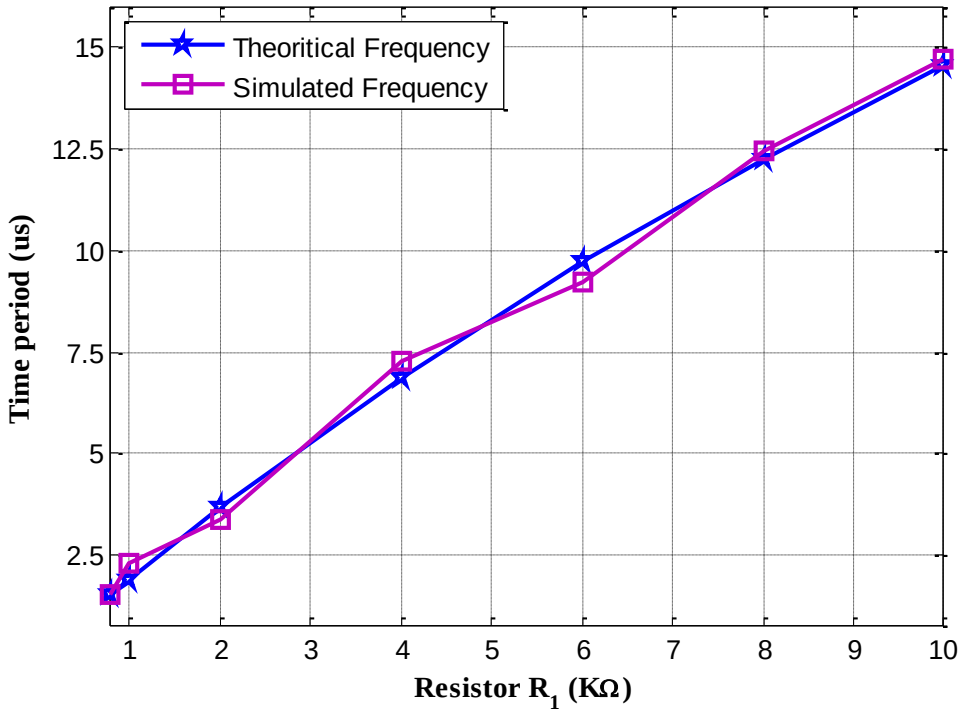


Fig. 8.24 Variation of time period against resistor R_1

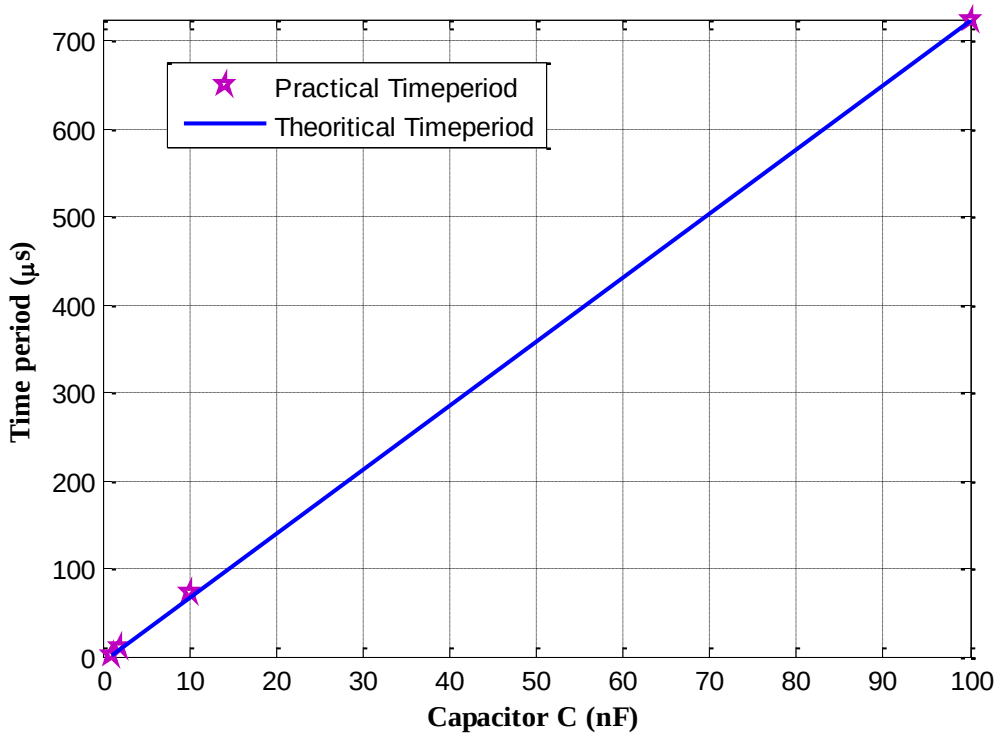


Fig. 8.25 Tunability against capacitor C

TABLE 8.2. Comparison of the proposed circuit in Fig. 4.8 (a) with the conventional square-wave generators in the literature

Square wave designs	Propsed design in Fig. 4.8(a)	Hou *et al.*2005 [45]	Chung *et al.*2005 [27]	Del re *et al.* 2007 [26]	Andrea *et al.* 2011 [25]	Pal *et al.* 2009 [18]	Srinivasulu 2011 [19]	Abuelmatti et al. 1998 [24]	Haque et al. 2008 [28]
No. of active components	1 OTRA	1 OTRA	3 OTA	1 CCII+	2 CCII+	2 CCII+	3 CCII+	1 CFOA	2 CFOA
No. of passive components	3 (1 Capacitor and 2 Resistors)	3 (1 Capacitor and 2 Resistors)	3 (1 Capacitor and 2 Resistors)	4 (1 Capacitor and 3 Resistors)	6 (1 Capacitor and 5 Resistors)	4 (1 Capacitor and 3 Resistors)	7 (1 Capacitor and 6 Resistors)	4 (1 Capacitor and 3 resistors)	5 (1 Capacitor and 4 Resistors)
No. of compo-nents	4	4	6	5	8	6	10	5	7
Maximum frequency range	3.33 MHz	12.5 MHz	16 kHz	2 kHz	737 kHz	260 kHz	574 kHz	71 kHz	60 MHz
Supply voltage	± 5 V	± 15 V	± 5 V	1.5 V (Integrate solution)	±15 V	± 5 V to ±15 V	± 6 V	Not available	± 5 V
Power consumption	182 mW	315 mW	> 1.8 W	750 µW (Integrate solution)	400 mW	384 mW	240 mW	Not available	Not available

For the tunability of resistor R_1, the selected passive component values are R_2 = 12 kΩ, C = 1 nF and R_1 is varied from 800 Ω to 10 kΩ. A linear variation of time period was exhibited by the circuit and it is presented in the form of plot in Fig. 8.24. Similarly, for the capacitor C, the selected parameter values are resistors R_1 = 15 kΩ and R_2 = 1.5 kΩ. The capacitor C is varied from 1 nF to 100 nF. The practical and theoretical time period variation against the capacitor C is plotted in Fig. 8.25.

Likewise, for the resistor R_2, the circuit is built with resistor R_1 = 15 kΩ, capacitor C = 1 nF and R_2 is varied from 200 Ω to 3 kΩ. The result is plotted in Fig. 8.26. From Figs. 8.24, 8.25 and 8.26, the variation of time period with respect to the passive components is linear. The comparative analysis of the proposed circuit shown in Fig. 4.8 (a) with the existing square wave generator circuits in the literature is shown in the Table 8.2.

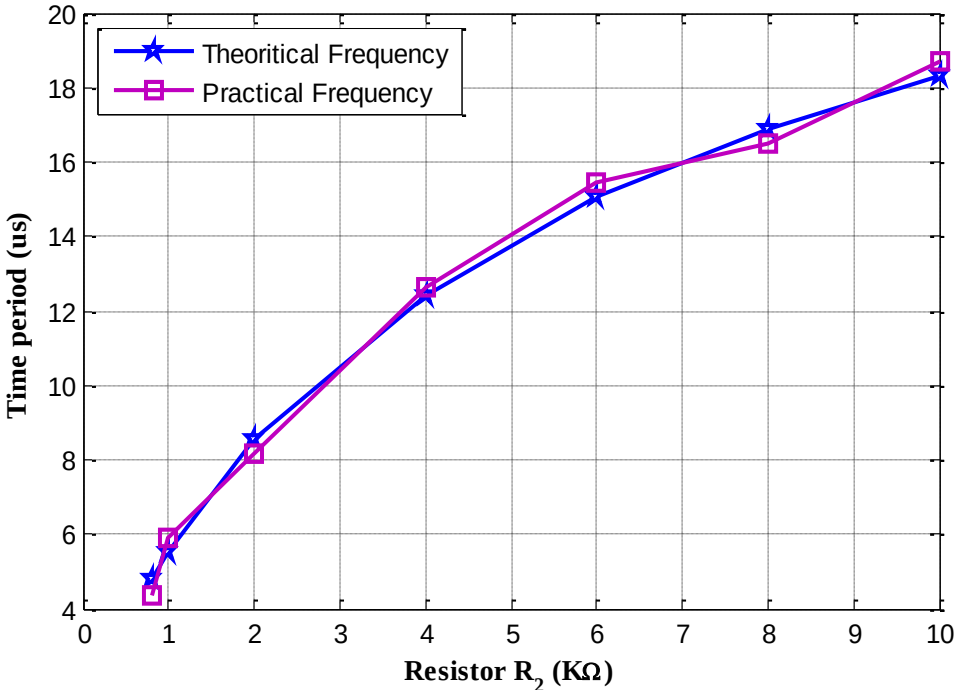


Fig. 8.26 Tunability against resistor R_2

The proposed circuits in Figs. 4.8 (a) and (b) will generate the waveforms independent of the resistor values and it exhibits more linear curve than the conventional OTRA square waveform generator circuits. The proposed circuits can generate the oscillations up to 3.33 MHz.

8.5 SUMMARY

In this chapter, experimental results are presented to validate the simulation analysis and theoretical analysis of the proposed circuits. All the proposed circuits are designed on a laboratory breadboard and corresponding output waveforms are presented in this chapter. The variation of oscillation frequency with respect to the passive components connected to the circuits is also presented for some circuits. For all the proposed circuits, experimental frequencies are matched with the simulated frequencies and the theoretically calculated frequencies.

CHAPTER 9

CONCLUSIONS AND SCOPE FOR FUTURE WORK

In this thesis, some novel waveform generators circuit design, operation and synthesis are presented. All the newly presented circuits in this thesis require a minimum number of active and passive components to generate the waveforms. The proposed sinusoidal oscillators, quadrature sinusoidal oscillators and square waveform generators are simulated using Spectre simulation model parameters and a repetition of them are carried on a laboratory breadboard using commercially available AD 844 AN ICs. All the practical and simulated results are correlated well with the theoretical analysis.

9.1. CONCLUSIONS

Chapter 1 construes the introductory overview of the importance of sinusoidal/ square waveform generators in electronic circuits and the evolution of active devices in waveform generation from voltage mode to the current mode. This chapter also includes the advantages derived by the current mode devices compared to the voltage mode devices.

In chapter 2, the main active device used for the design and implementation of waveform generators is given. The CMOS implementations of the OTRAs given in [32, 33] are used for waveform generation. The CMOS OTRA structures are redesigned using Cadence CMOS gpdk 180 nm technology and simulated using Spectre simulation model parameters. The CMOS transistors W/L ratios are given. The simulated output voltage variation with respect to the input terminal currents is given. The variation of input and output terminal's resistances are also presented in the form of figures. The simulated DC open-loop transresistance gain of the OTRAs is also presented in this chapter. In order to validate the proposed circuits, the OTRA is implemented on laboratory breadboard by using commercially available ICs AD 844 AN. The OTRA implementation using two AD 844 AN ICs and a resistor are given in this chapter.

Chapter 3, mainly focuses on the existing applications and waveform generators have been designed using OTRA. This chapter also provides detailed analysis and important issues involved in the design and implementation of the waveform generators by using OTRA. Each subsection related to the waveform generators by using OTRA also provides intermediate conclusions concerned with the (merits and demerits) advantages and disadvantages posed by the available OTRA based waveform generators in the literature.

Chapter 4-8 presents the main objective of the thesis. Novel active sinusoidal oscillators, quadrature sinusoidal oscillators and square waveform generators are designed in chapter 4. The operation of the proposed waveform generators is discussed in this chapter. Based on the literature survey and the importance of the sinusoidal oscillator in the field of electronics, a generalized configuration using single OTRA with a grounded passive component(s) is proposed in this chapter. Several oscillator circuits can be generated by using the proposed generalized configuration. The minimum passive component sinusoidal oscillator circuit with four passive components is generated by using the generalized configuration. Twelve special case oscillator circuits by using the generalized configuration are presented in this chapter. In these oscillator circuits, seven oscillator circuits are having a single grounded resistance.

The grounded resistance in these oscillator circuits can be replaced with a grounded capacitor. The condition of oscillation and frequency of oscillation can be controlled independently in most of the oscillator circuits realized from the generalized configuration. Two special case oscillator circuits with grounded resistance and capacitance are also presented in this chapter. In these two oscillator circuits, the condition of oscillation and frequency of oscillation are controlled independently. In all the proposed circuits, the grounded resistance/capacitance can be replaced with a JFET to realize a voltage controlled oscillator. Two quadrature sinusoidal oscillator circuits using two OTRAs along with a few passive components are also presented in this chapter. The condition of oscillation and frequency of oscillation can be controlled independently in the proposed quadrature sinusoidal oscillators.

Two square waveform generators are presented in this chapter. The first square waveform generator is designed with one OTRA, two resistors and a capacitor. This square waveform generates fixed and almost equal on-duty and off-duty cycles. The

output waveform time period can be varied by any of the passive components connected to the circuit. This circuit makes a linear variation of the time period with respect to the passive components connected to the circuit. The second square waveform generator circuit presented in this chapter can be able to vary both the on-duty and off-duty cycles at a time. This circuit is designed with one OTRA, two diodes and four passive components. By varying the passive component values, the on-duty and off-duty cycles can be adjusted to the required time period. The operation of the square waveform generators to oscillate between the positive saturation to the negative saturation levels is depicted in this chapter.

In chapter 5, the mathematical derivations for the circuits presented in chapter 4 are given. A generalized configuration is implemented to realize ten sinusoidal oscillator circuits presented in chapter 4. From this generalized configuration a generalized characteristic equation is derived by considering the admittances of the passive components connected to the generalized configuration. The characteristic equation for the proposed generalized configuration is derived by considering the ideal behavior of the OTRA. The condition of oscillation and frequency of oscillation for all the newly proposed oscillator circuits can be derived from the generalized characteristic equation.

The characteristic equation can also be derived independently for all the sinusoidal oscillator circuits without depending on the generalized characteristic equation. Similarly, for the two quadrature sinusoidal oscillator circuits presented in chapter 4, the characteristic equation is derived by applying the general network laws to the circuits. The last subsection in this chapter describes the mathematical analysis of the two square waveform generators proposed in chapter 4. By considering the ideal behaviour of the OTRA, the mathematical derivation for the time period of the proposed square waveform generators is carried out. The output waveform of the square waveform generator has two saturation levels. The output waveform changes its state when the inverting input terminal current is more than the non-inverting input terminal current of the OTRA and vice versa.

In chapter 6, the non-ideal analysis of the waveform generators, presented in chapter 4, is described. All the proposed circuits presented in chapter 4 and their derivations for frequency or time period given in chapter 5 is re-analysed by considering the non-ideal model of the OTRA. In OTRA, the output voltage is the

difference of two input terminal currents multiplied by the transresistance gain R_m, which is ideally infinite. The inverting and non-inverting input terminals of the OTRA are internally grounded. The parasitic capacitances and resistances (R_p, R_n and R_0) associated with the input and output terminals of the OTRA are very small, grounded and negligible. Thus the most important non-ideality in OTRA is due to the finite transresistance gain R_m. The finite transresistance gain R_m along with the frequency limitations associated with the OTRA must be considered in the analysis of the OTRA based circuits. The equivalent non-ideal model of the OTRA implemented with the ICs AD 844 is also discussed in this chapter. This equivalent OTRA model is redesigned by considering the finite parasitic resistances and non-zero current tracking errors.

In chapter 7, the simulation results for the newly proposed circuits in chapter 4 are given. All the proposed circuits are designed with the CMOS OTRA realization given in chapter 2 along with a few passive components. The proposed circuits in chapter 4 are simulated by using Spectre simulation model parameters with a supply voltage of ± 1.8 V. The sinusoidal oscillator circuits realized from the generalized configuration are designed with appropriate passive component values, to satisfy the condition of oscillation, to produce the sinusoidal output waveform. The simulated output waveforms of the proposed circuits along with passive component values are given to validate the theoretical analysis. Similarly, for the quadrature sinusoidal oscillator circuits the passive components are chosen to produce the oscillations at the output terminals of the OTRAs. All the sinusoidal and quadrature sinusoidal oscillators are tested with different passive component values to satisfy the barkhausen criterion to produce sustained oscillations at the output terminal of the OTRA. The simulated results are in good agreement with the mathematical analysis given in the previous chapter.

Two new square waveform generators are proposed in chapter 4. The first one is the fixed duty cycle square waveform generator, i.e. the on-duty and off-duty cycles are fixed and almost equal with this circuit. The second circuit is able to vary the duty cycles to the required time period. For producing the square waveform in the proposed square waveform generators, the required time period is chosen first. Then the passive component values are arbitrarily determined from the time period equation

derived in chapter 5. The capacitor and resistance values can be tuned to select the required time period or frequency. The second square waveform generator is also called as a variable duty cycle waveform generator. In this waveform generator the resistance values are chosen to select the on-duty cycle time period, which is more than the off-duty cycle time period. These resistance values will be reversed if the off-duty cycle time period is more than the on-duty cycle time period. The simulated output waveforms are matched well with the theoretical analysis given in the previous chapter.

This chapter aims at the workability of the new topologies proposed in chapter 4. All the circuits presented in this thesis are experimentally checked for waveform generation using a laboratory breadboard. The prototype OTRA realization by using two AD 844 ICs shown in chapter 2 has been used to validate the theoretical and simulation analysis with the hardware results. The IC AD 844 is a high speed monolithic current feed-back operational amplifier (CFOA). This IC is very popular by its applications in current-mode circuits. The oscillator circuits generated from the generalized configuration are connected on the laboratory breadboard for testing the waveform generation and frequency tuning.

The passive components used for generating sinusoidal oscillations and frequency tuning are given to validate the theoretical analysis. For all measurements on laboratory breadboard the supply voltage of ± 5 V is used. The photographic pictures of the output waveforms on the oscilloscope screen are shown in this chapter. The percentage of errors between the theoretical frequencies and experimental frequencies are given for the oscillator circuits. The circuits having the advantage of tuning independently over the condition of oscillation and frequency of oscillation are tuned with respect to the passive component.

The frequency tuning of such circuits is presented in the form of figures. For frequency tuning, one of the passive components connected to the circuit is varied over a range while the other passive components are kept constant. The comparison of the proposed oscillator circuits realized from the generalized configuration with the existing oscillator circuits from the literature in terms of number of active and passive components, supply voltage and power consumption to produce the waveform is presented in this chapter. Similarly, the quadrature sinusoidal oscillator circuits are

also implemented and checked for waveform generation using a laboratory breadboard. The output waveform in the oscilloscope and frequency tuning with respect to the passive components are presented in the form of plots.

For generating the square waveform in the square waveform generators proposed in chapter 4 the required time period is chosen first. Then the passive component values could be calculated from the time period equation shown in chapter 5. The experimental output waveforms of the square waveform generators are shown to validate the mathematical analysis and simulation analysis. The time period tuning with respect to the passive components is presented in the form of plots. From these plots, the time period curve is more linear than the existing OTRA based square waveform generator. The comparison of the proposed square waveform generator with the conventional OTRA based square waveform generator is given in terms of number of active components, number of passive components, maximum frequency range, supply voltage and power consumption to produce the square waveform.

9.2. SCOPE FOR FUTURE WORK

Further work can be done by implementing the OTRA in sub-microvolt region to decrease the supply voltage and power consumption. The OTRA can be implemented using FinFET, TFET and HTFET to achieve the low power consumption with low supply voltage.

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